

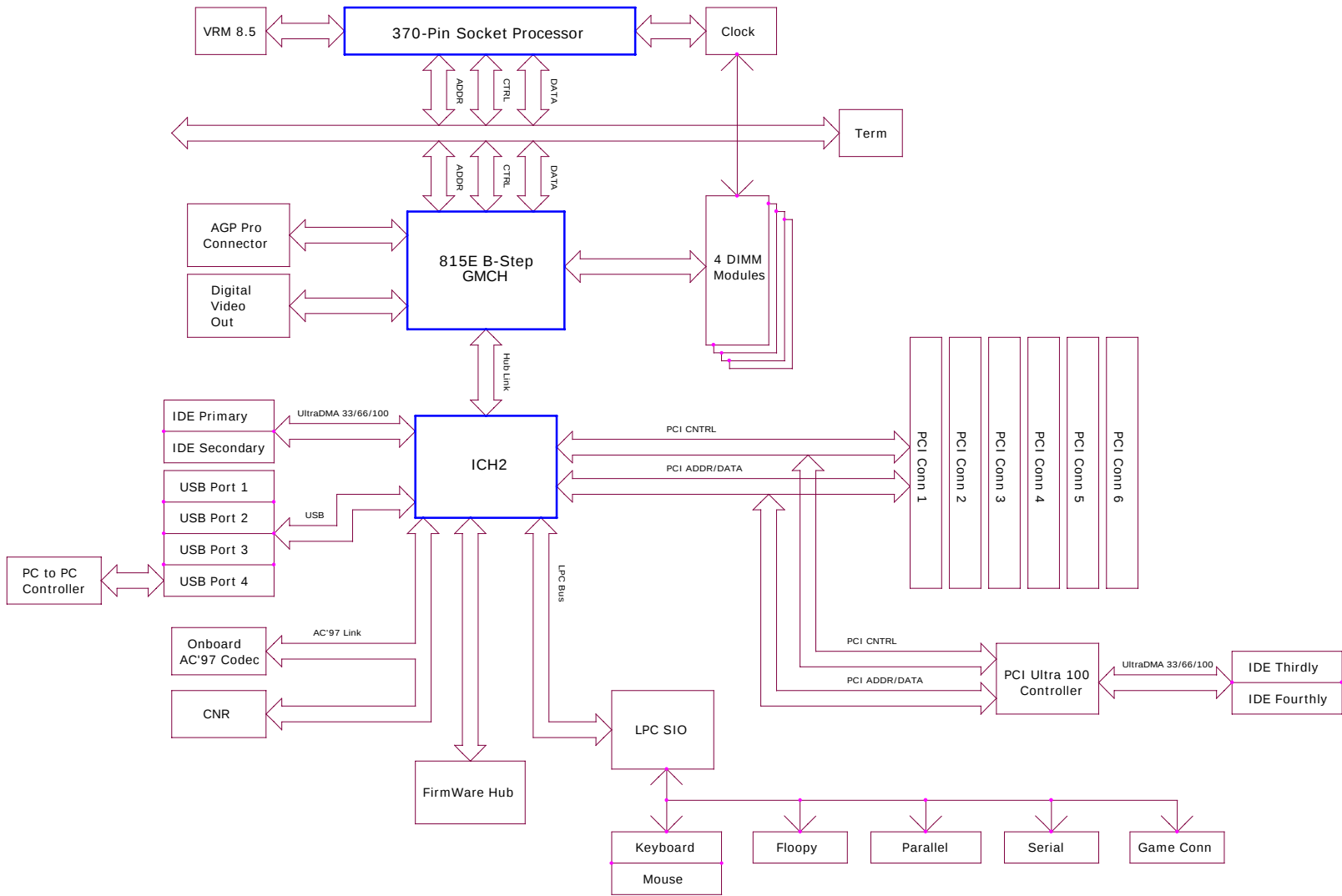
MS-6337 ATX

Revision 5.0B

Intel PGA 370 Processor
Intel 815E B-Step Chipset
Winbond 83627HF-AW LPC I/O
PROMISE PDC20265 PCI Ultra 100 Controller
Genesys USB PC to PC Networking Controller

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Block Diagram



General Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	PREQ#5 (multifunction pin)
GPIO 2	I	Pull up through 2.7K ohms (PIRQE#)
GPIO 3	I	Pull up through 2.7K ohms (PIRQF#)
GPIO 4	I	Pull up through 2.7K ohms (PIRQG#)
GPIO 5	I	Pull up through 2.7K ohms (PIRQH#)
GPIO 6	I	Primary IDE ATA66/100 detection (ATADET0)
GPIO 7	I	Secondary IDE ATA66/100 detection (ATADET1)
GPIO 8	I	Pull Up to 3.3VSBY through 10K ohms (LAN Wake Up)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntn pin)
GPIO 12	I	Pull Up to 3.3VSBY through 4.7K ohms (External SMI)
GPIO 13	I	Pull Up to 3.3VSBY through 4.7K ohms (LPC PME)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	PGNT#5 (multifuntn pin)
GPIO 18	O	Pull down through 8.2K ohms (unused)
GPIO 19	O	accomplished with GPIO20 for DIMM voltage
GPIO 20	O	accomplished with GPIO19 for DIMM voltage
GPIO 21	O	Pull Up to 3.3V through 4.7K ohms (Vcore Setting)
GPIO 22	OD	Pull Up to 3.3V through 4.7K ohms (A20M# Control)
GPIO 23	O	Pull Up to 3.3V through 4.7K ohms (BIOS protect)
GPIO 24	I/O	Pull Up to 3.3VSBY through 4.7K ohms (STR Control)
GPIO 25	I/O	Pull Up to 3.3VSBY through 4.7K ohms (KBVCC Control)
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	Pull Up to 3.3V through 4.7K ohms (Audio Control)
GPIO 28	I/O	CNR Detected
GPIO 29~31	O	Not Implemented

VCC3STR	GPO19	GPO20
3.3V	1	1
3.4V	0	1
3.5V	1	0
3.6V	0	0

BIOS Protect Config.	GPIO23
BIOS Un_Protected	1
BIOS Protected	0

VCORE Setting	GPIO21
CPU Default	1
Maanuel Setting	0

STR Control Config.	GPIO24
Power Off	X
Power On / Disable	1
Before Enter S3	0

A20M# Config.	GPIO22
A20M# used	1
A20M# unused	0

KBVCC Config.	GPIO25
KB Power On Enable	1
KB Power On Disable	0

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull up through 1K ohms (unused)
GPI 2	I	GPI2 = 0 GPI3 = 1 ; Flash from FDD
GPI 3	I	GPI2 = 1 GPI3 = 0 ; Boot Auto clear CMOS
GPI 4	I	Pull up through 1K ohms (unused)

LPC

GPIO Pin	Type	Function
GPIO 24	I/O	Pull Up to 5V through 22K ohms (DLED2)
GPIO 32	I/O	Pull Up to 5V through 22K ohms (DLED1)
GPIO 33	I/O	Pull Up to 5V through 22K ohms (DLED4)
GPIO 34	I/O	Pull Up to 5V through 22K ohms (DLED3)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK1	13 (PCI1/FS1)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK2	14 (PCI2/SEL24_48#)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK3	17 (PCI3)
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19	PCICLK4	18 (PCI4)
PCI Slot 5	INTA# INTB# INTC# INTD#	AD20	PCICLK5	19 (PCI5)
PCI Slot 6	INTB# INTC# INTD# INTA#	AD21	PCICLK6	20 (PCI6)
Ultra 100	INTB#	AD25*	ATAPCLK	14 (PCI2/SEL24_48#)

* ICH2 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

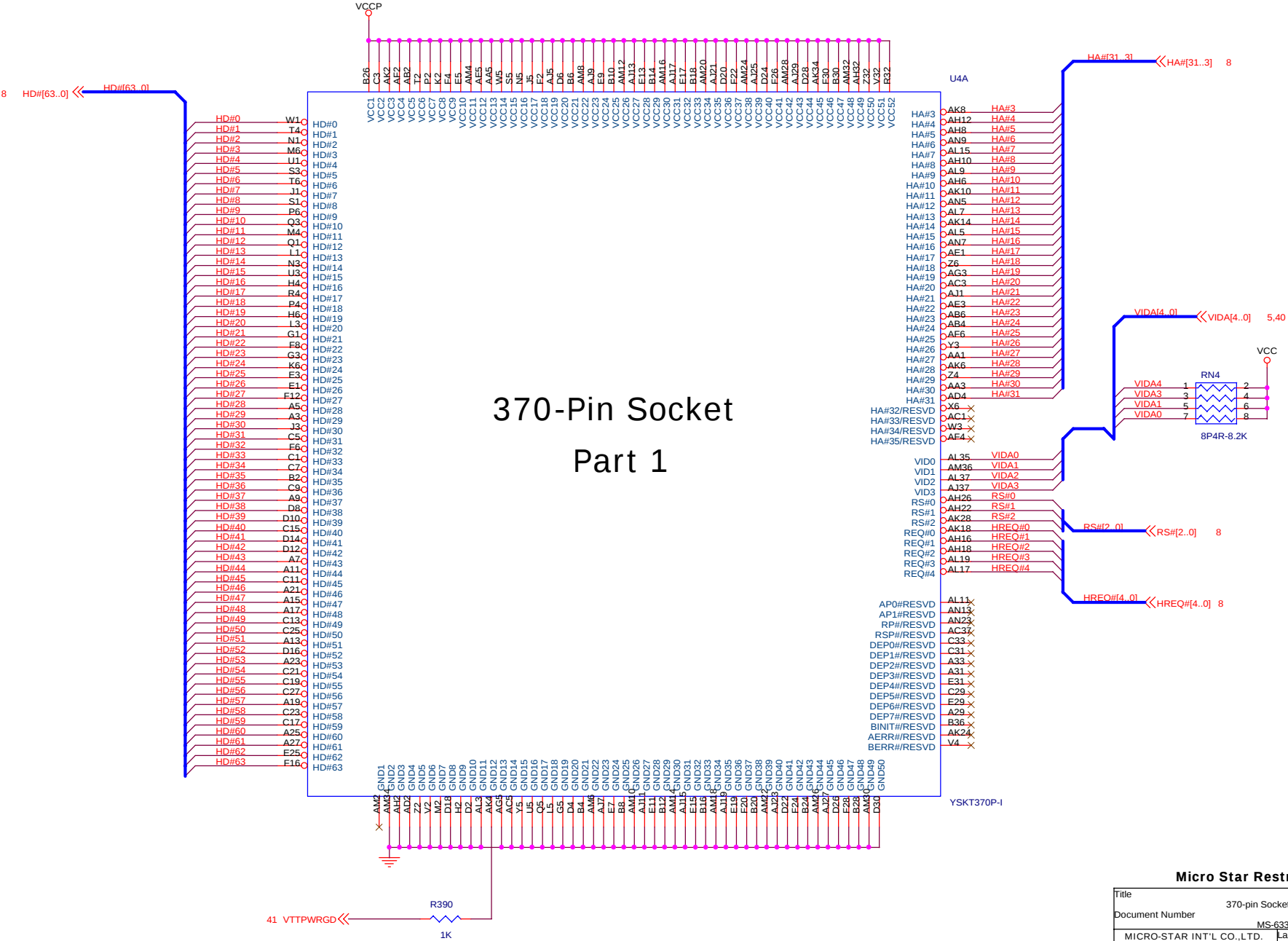
DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK4 DCLK5 DCLK0 DCLK1
DIMM 2	1010001B	DCLK11 DCLK9 DCLK2 DCLK3
DIMM 3	1010010B	DCLK8 DCLK10 DCLK7 DCLK6
DIMM 4	1010011B	DCLK10 DCLK8 DCLK6 DCLK7

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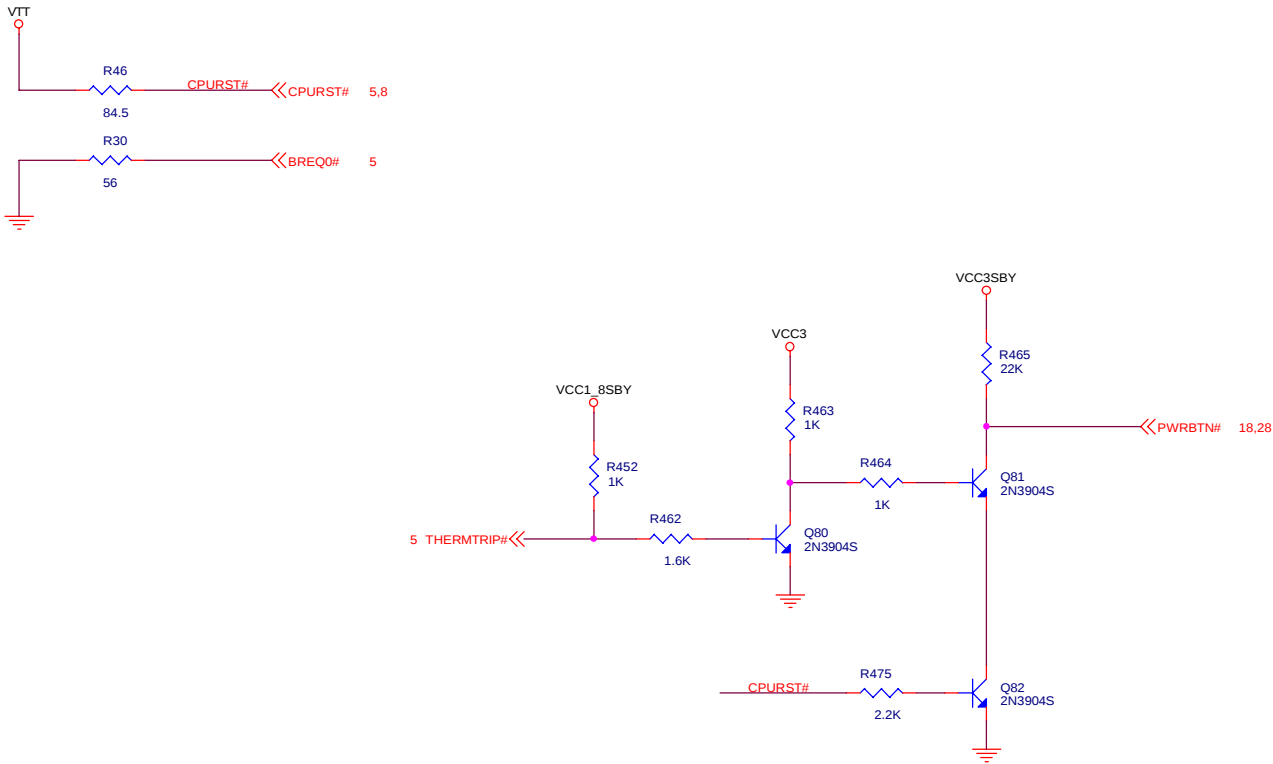
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370PGA Socket Part 1



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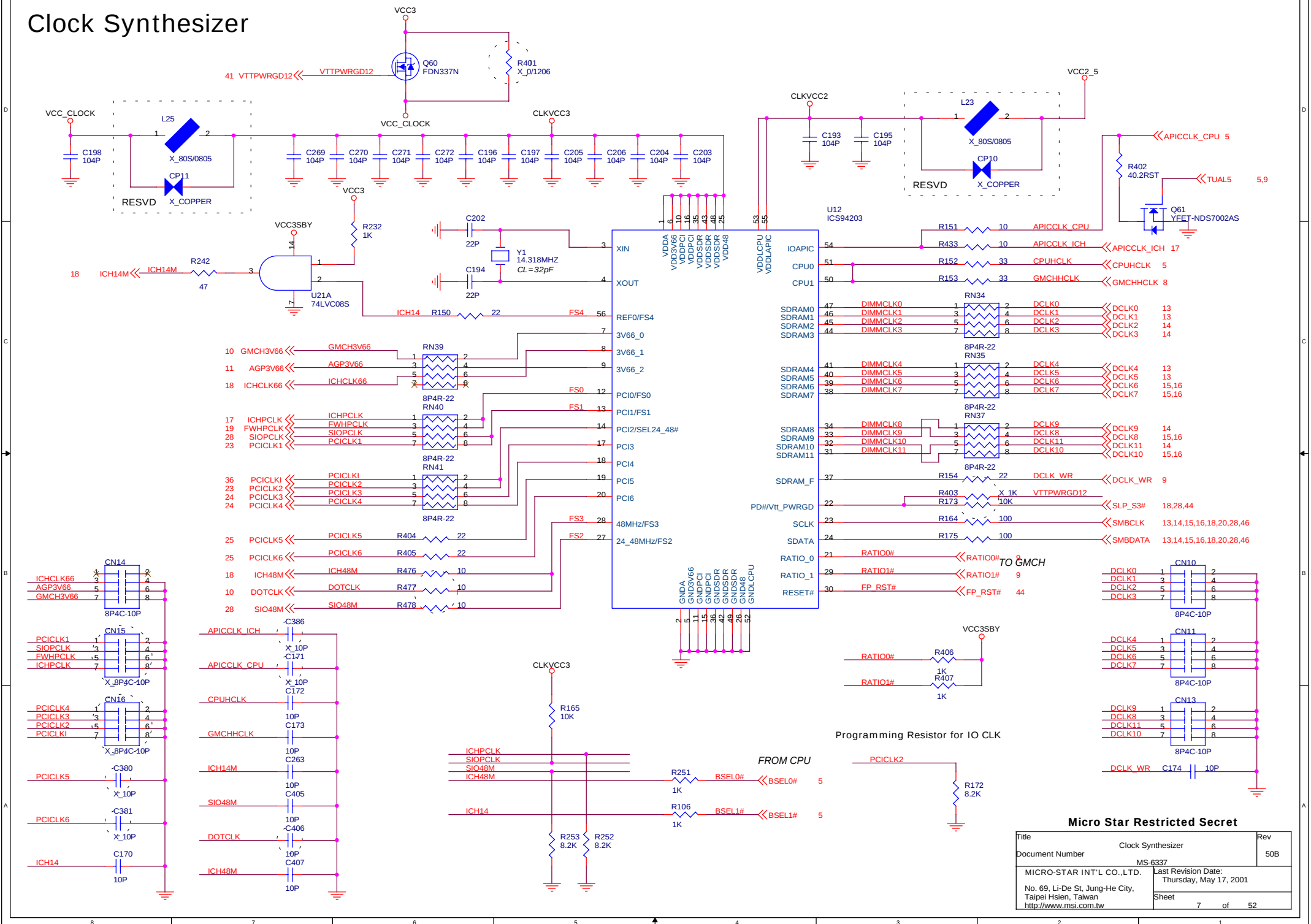
AGTL Termination and Thermtrip#



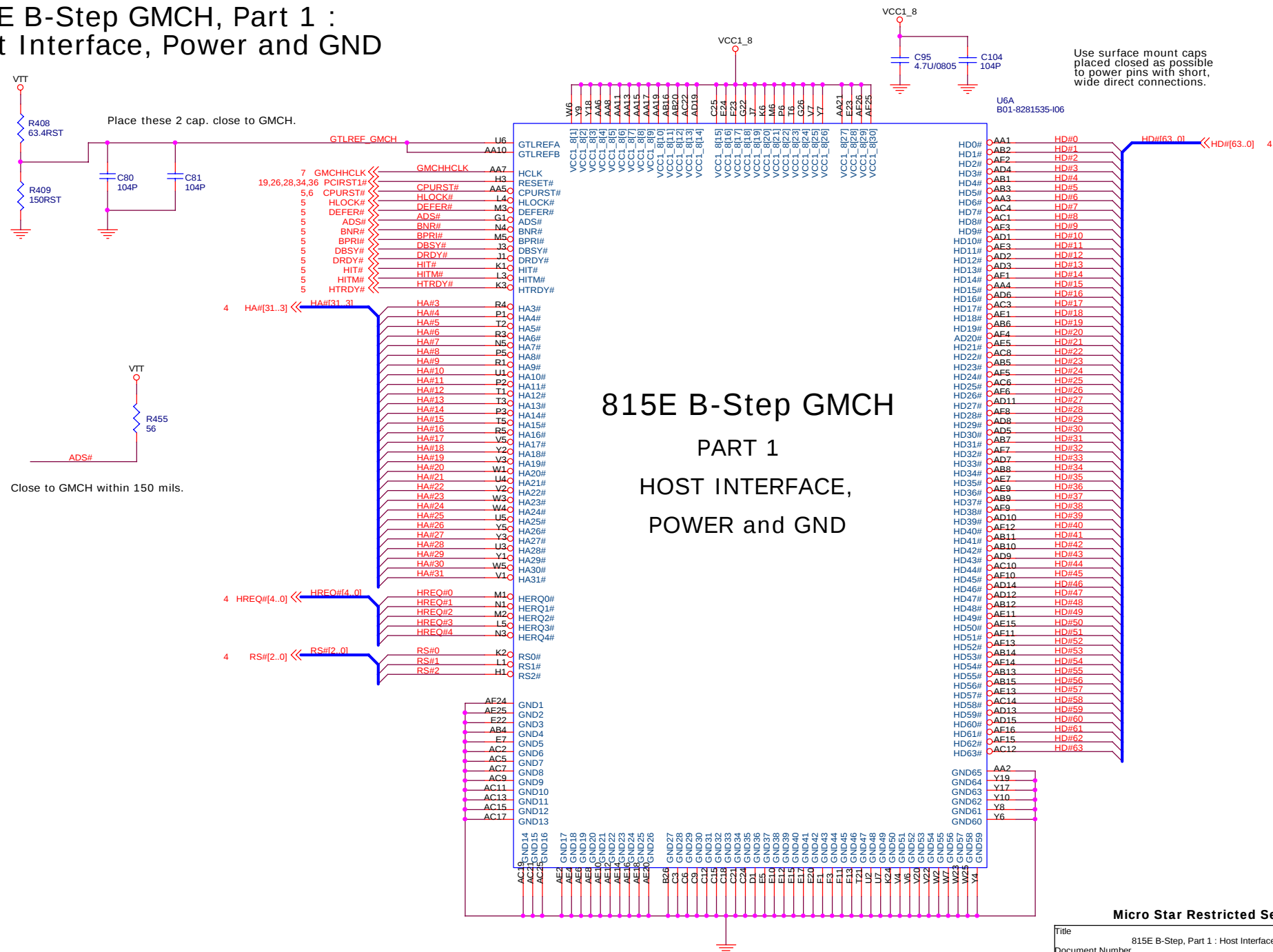
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Clock Synthesizer



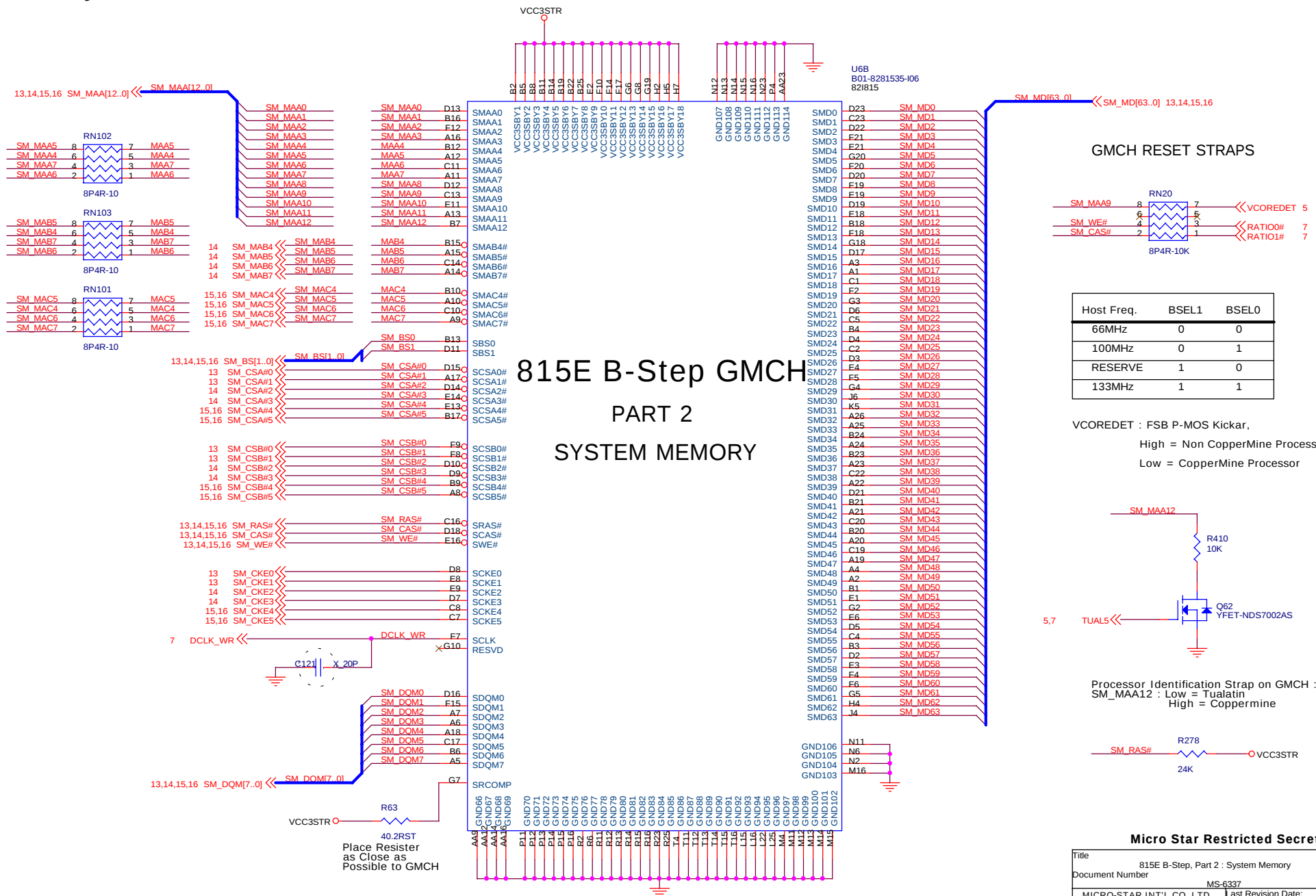
815E B-Step GMCH, Part 1 : Host Interface, Power and GND



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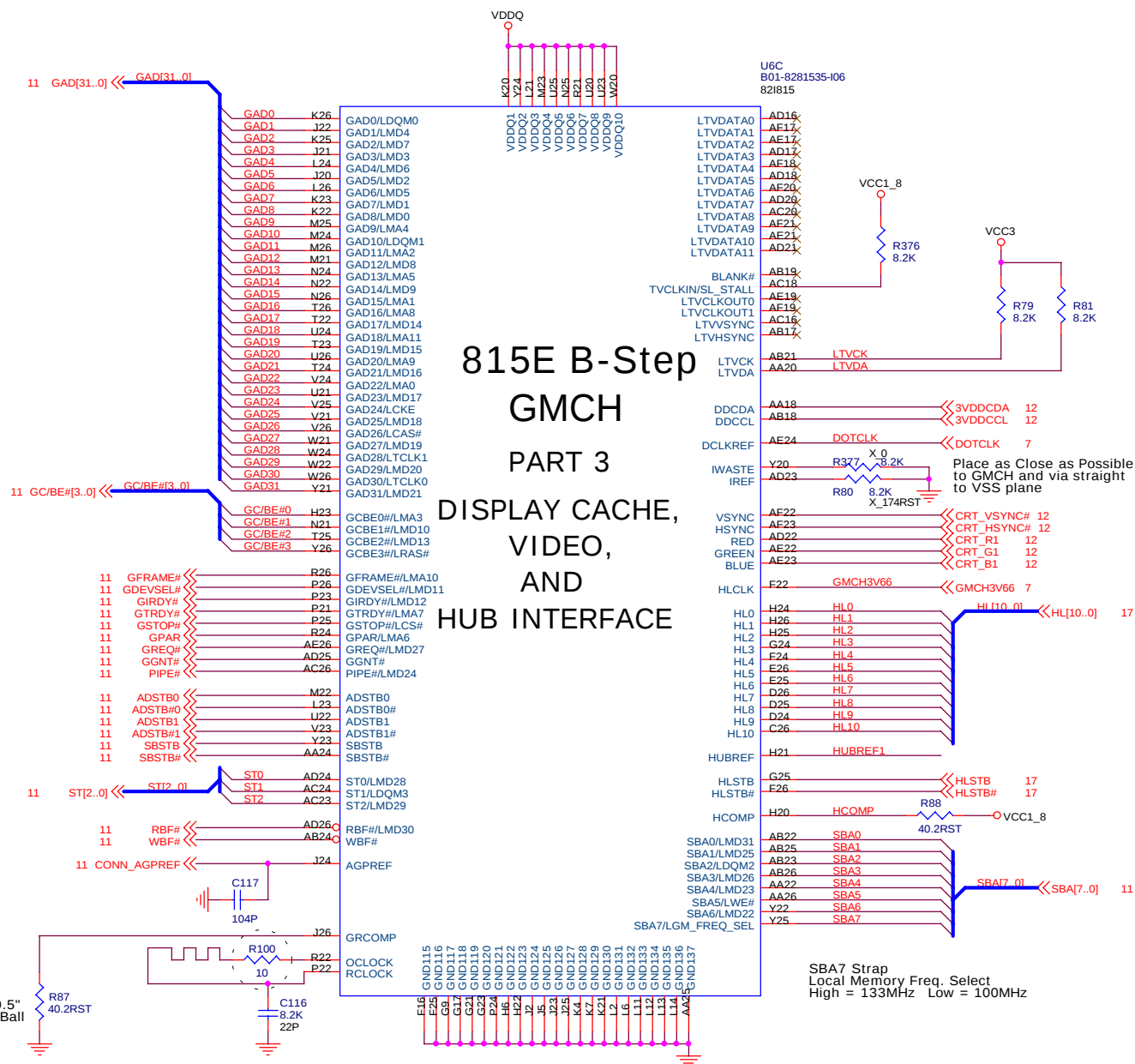
815E B-Step GMCH, Part 2 : Memory Interface



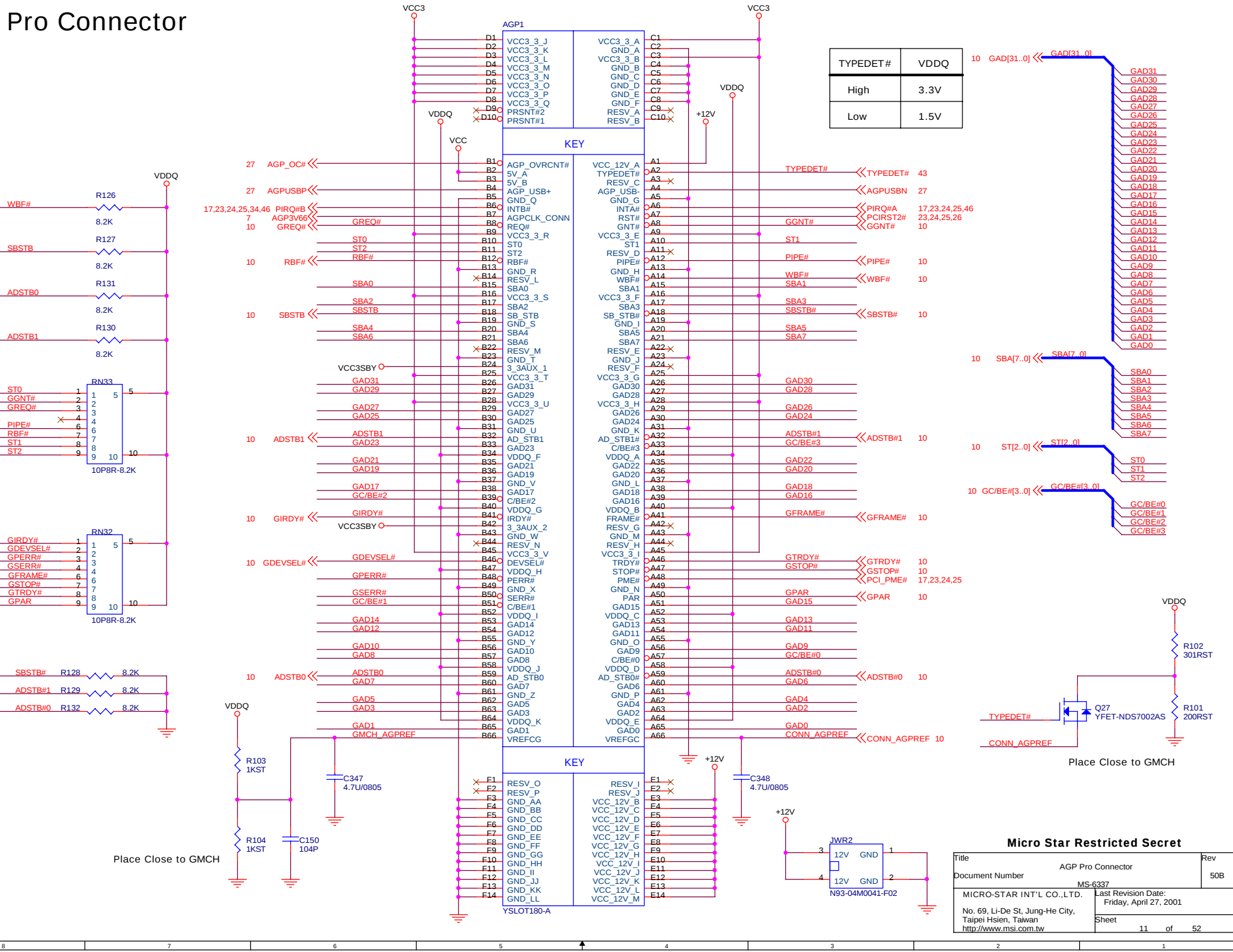
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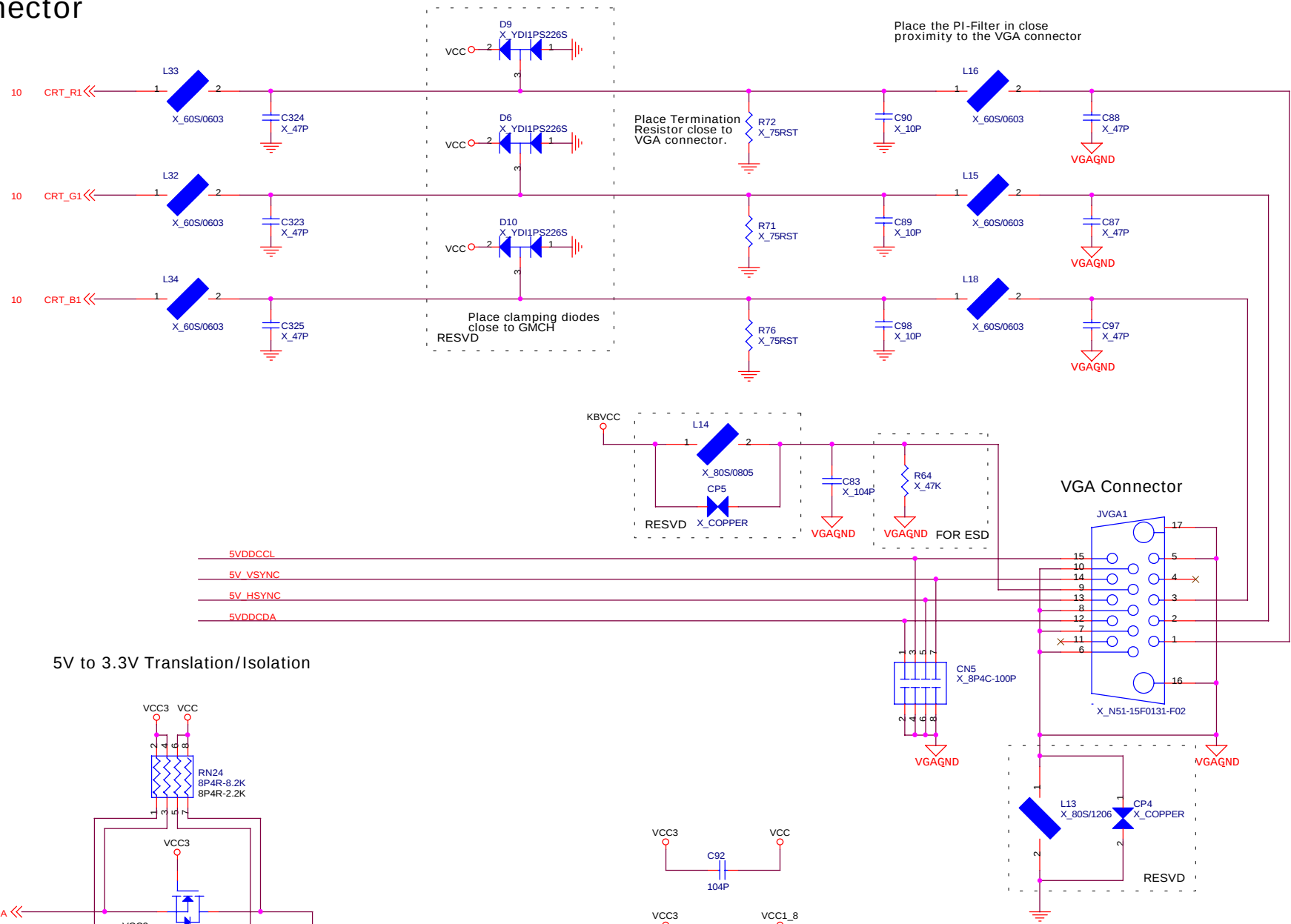
815E B-Step GMCH Part 3 : AGP/Display Cache, Video and HUB Interface



AGP Pro Connector

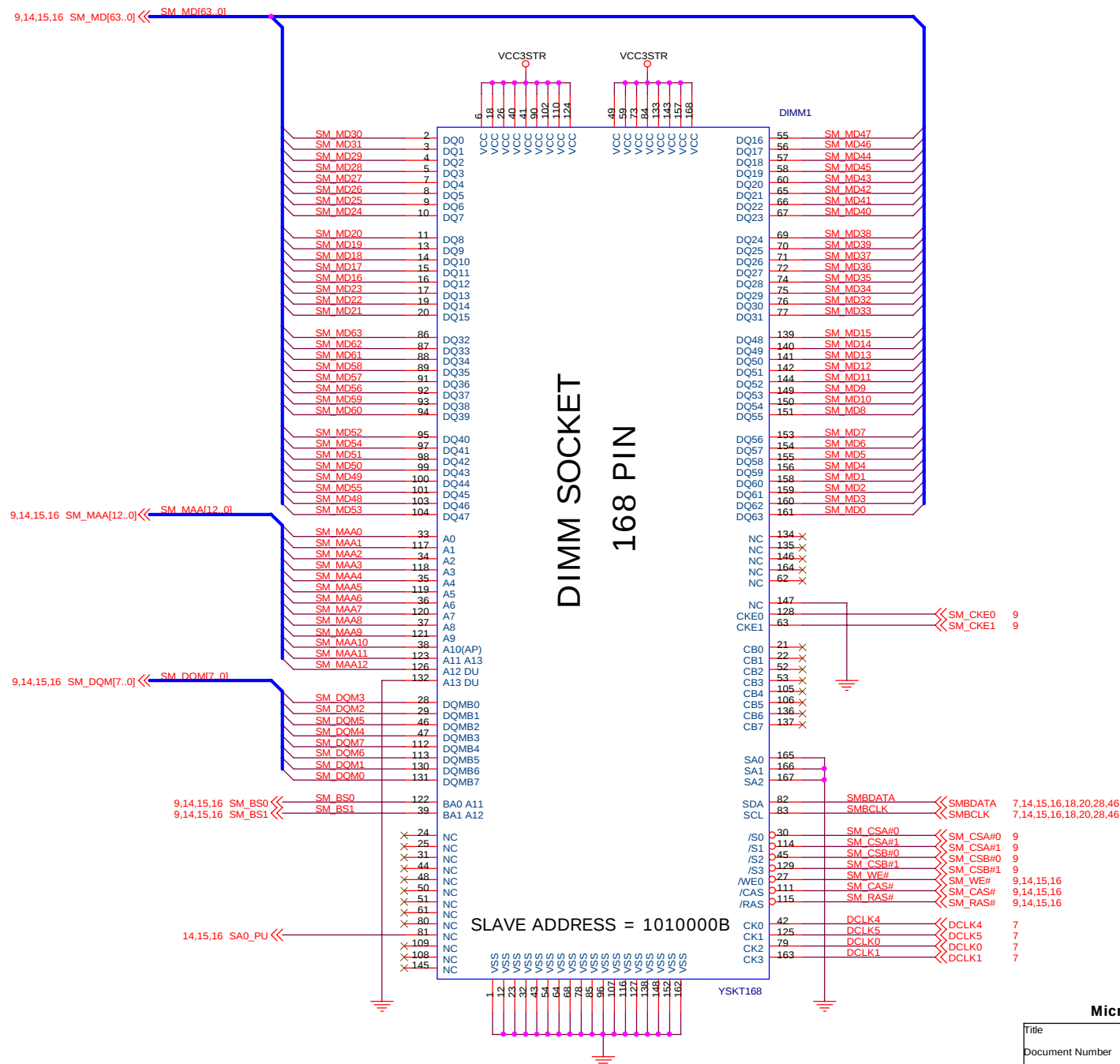


Video Connector



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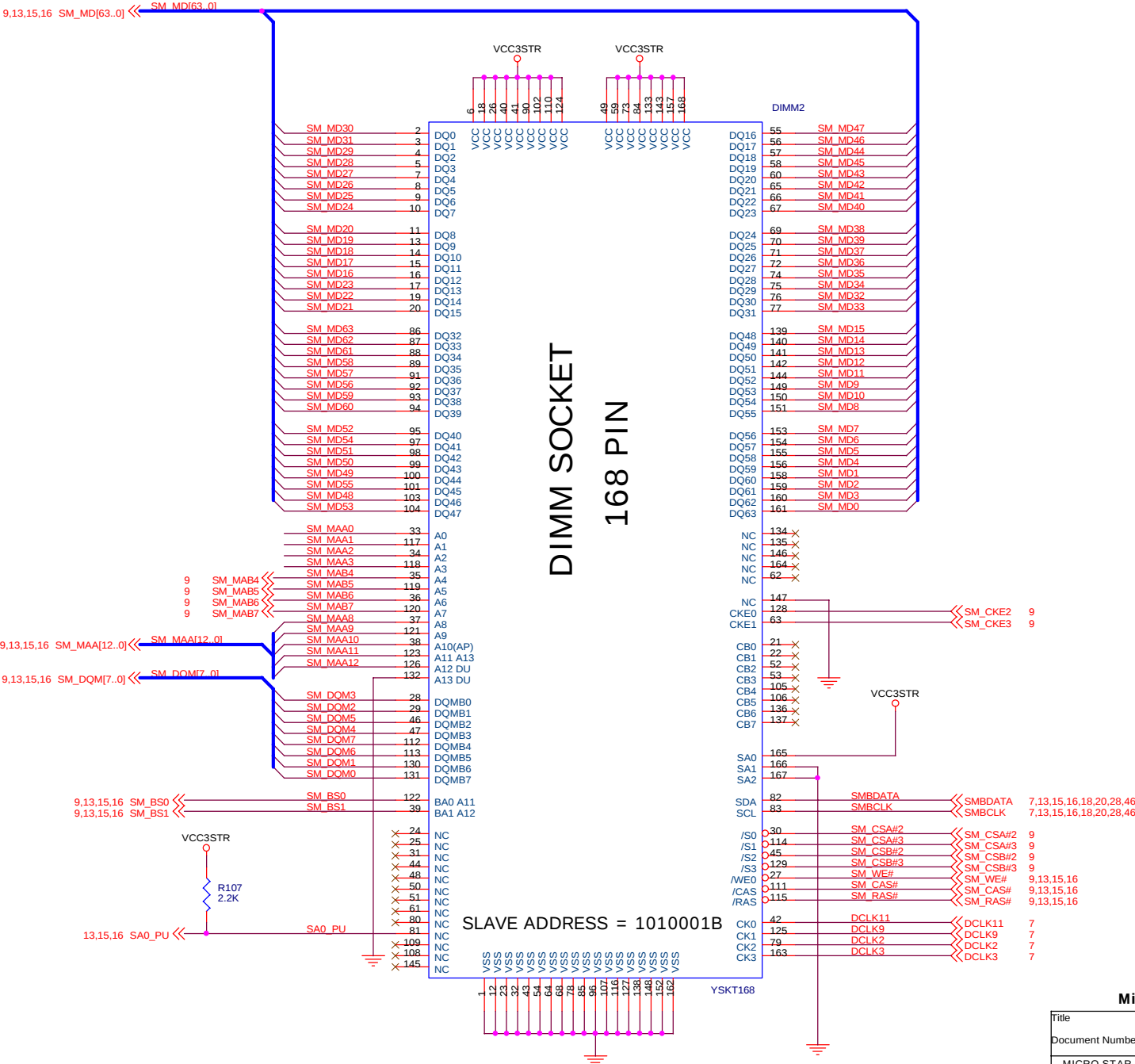
SYSTEM MEMORY



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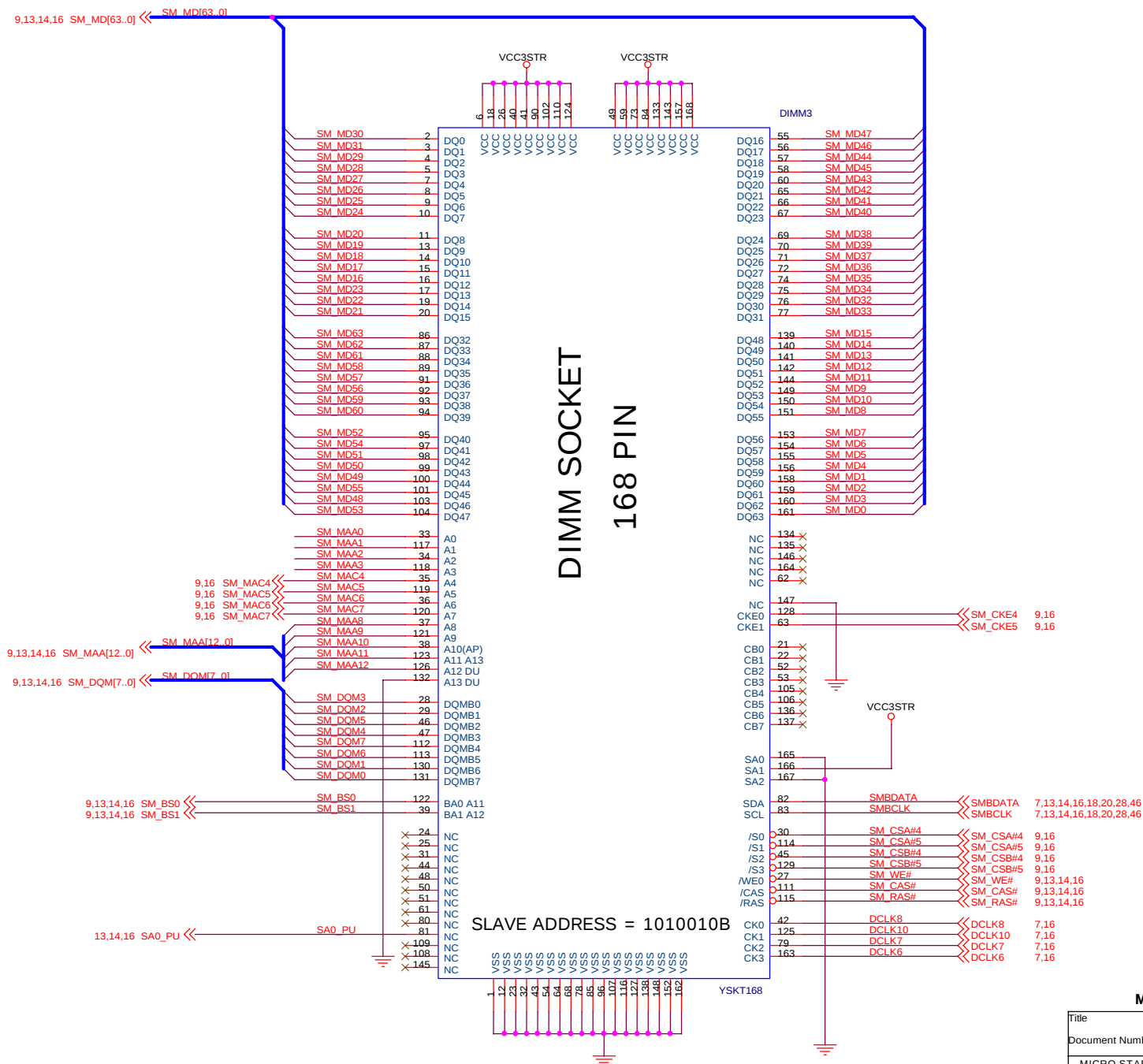
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SYSTEM MEMORY



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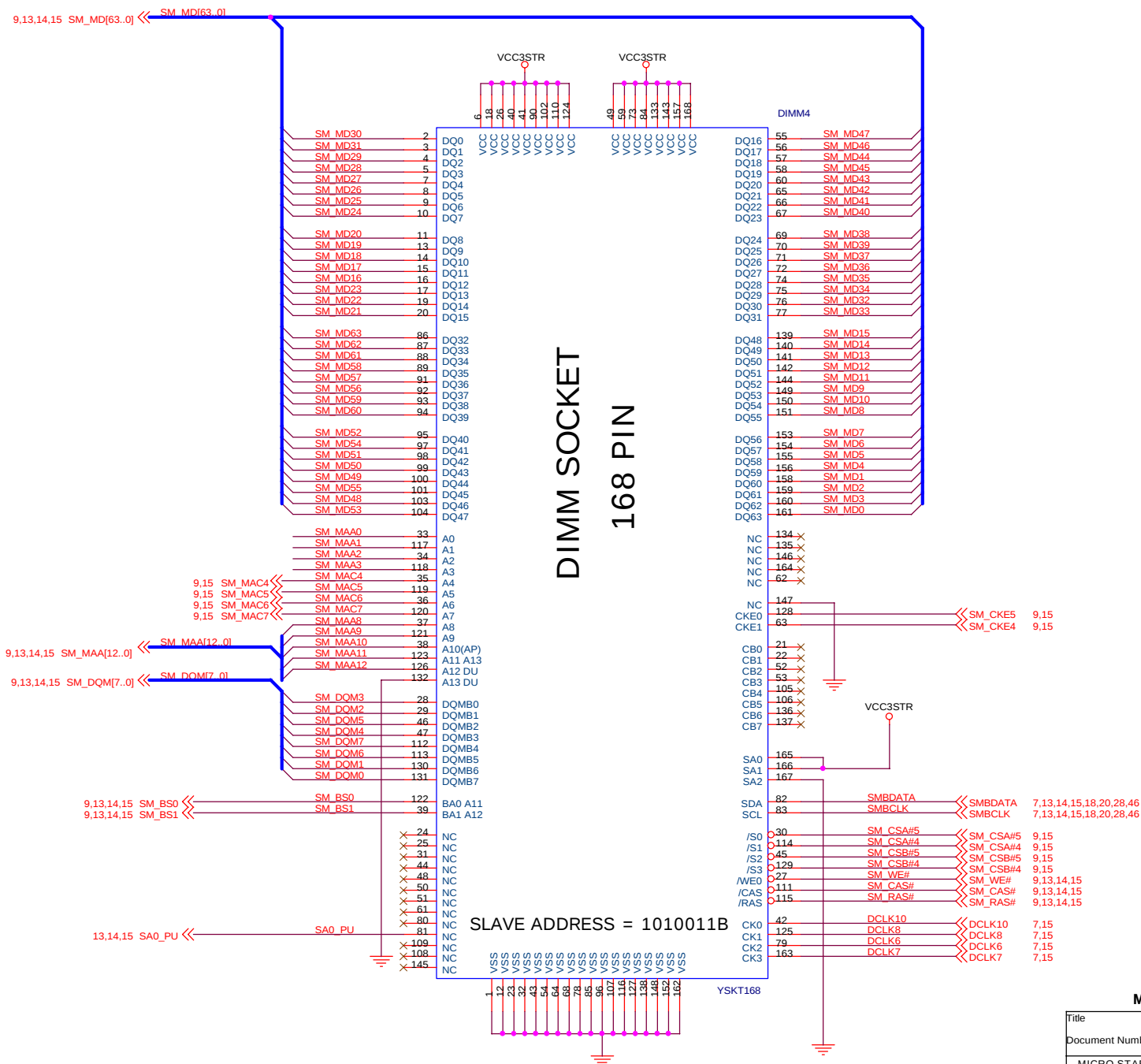
SYSTEM MEMORY



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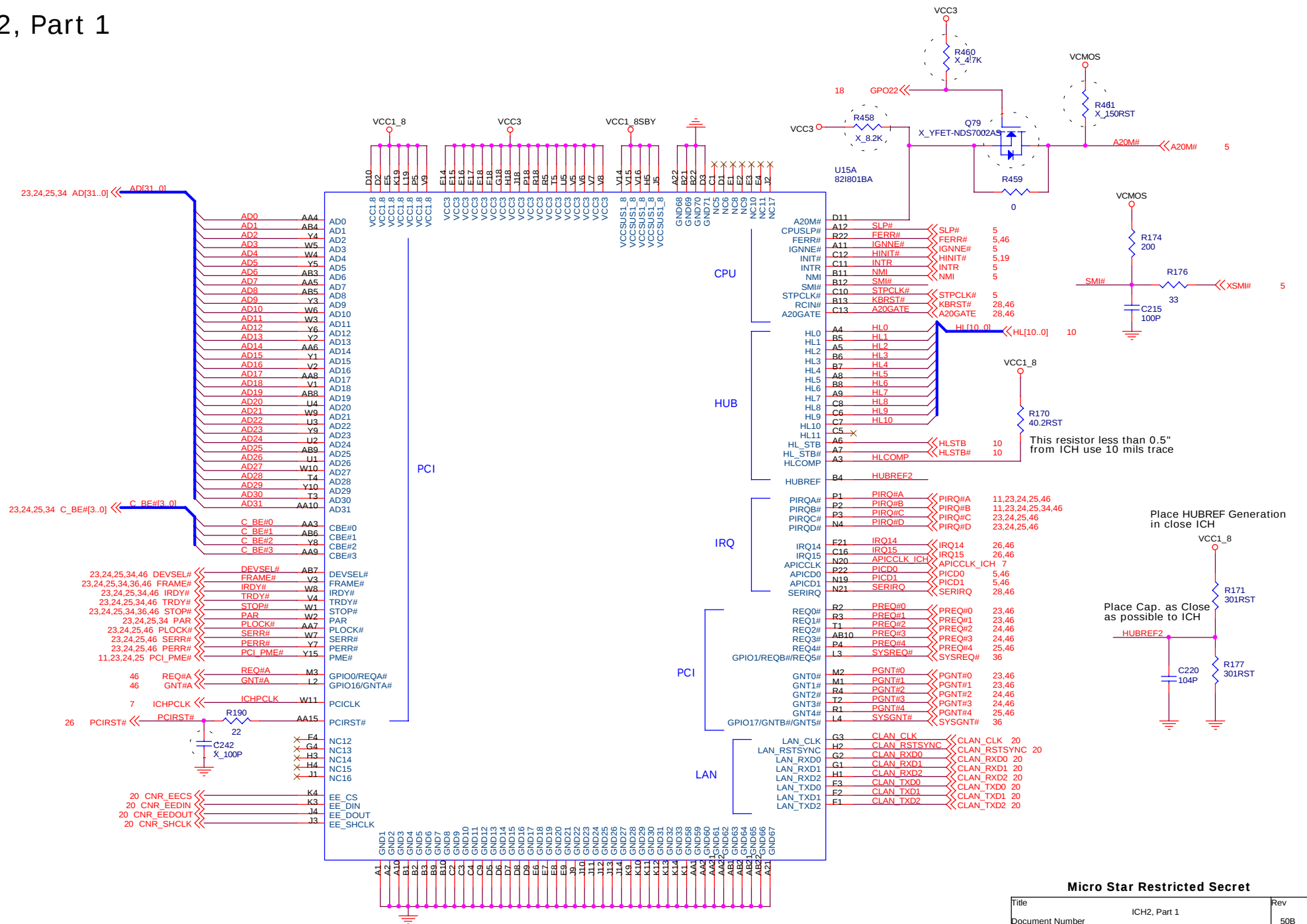
SYSTEM MEMORY



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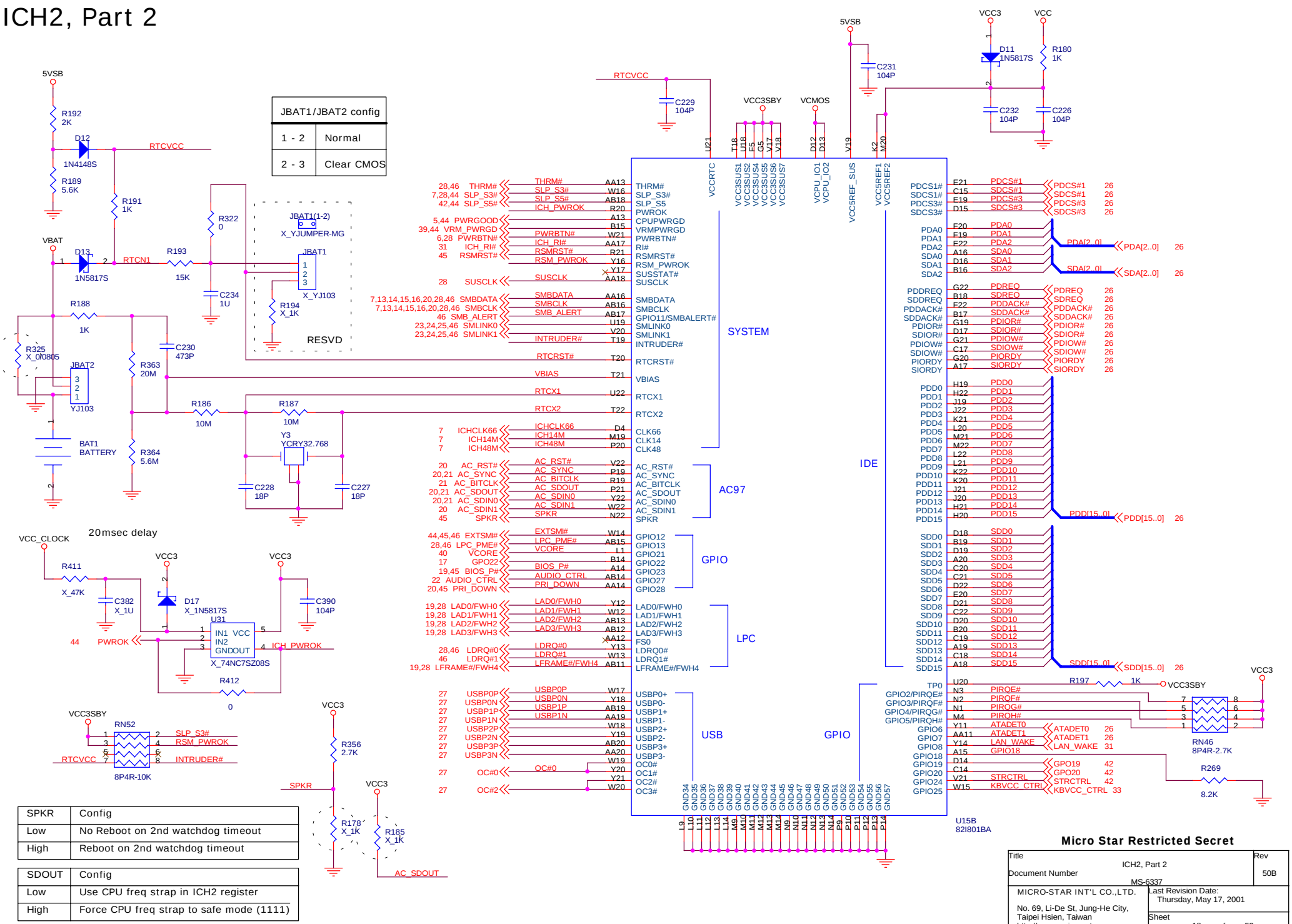
ICH2, Part 1



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ICH2, Part 2



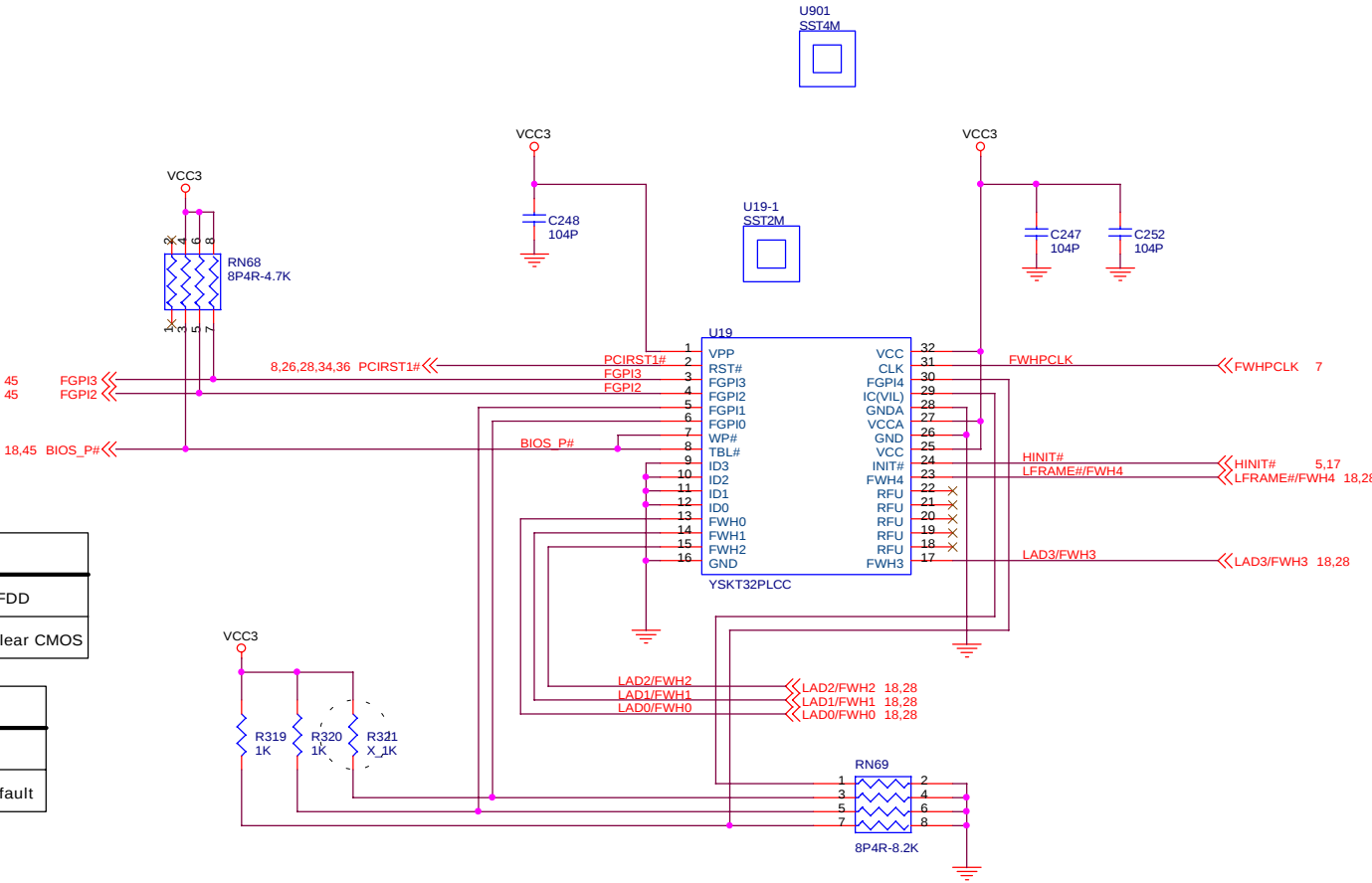
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Firmware Hub (FWH)

GPI2	GPI3	Config.
LOW	HIGH	Flash from FDD
HIGH	LOW	Boot auto clear CMOS

BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default



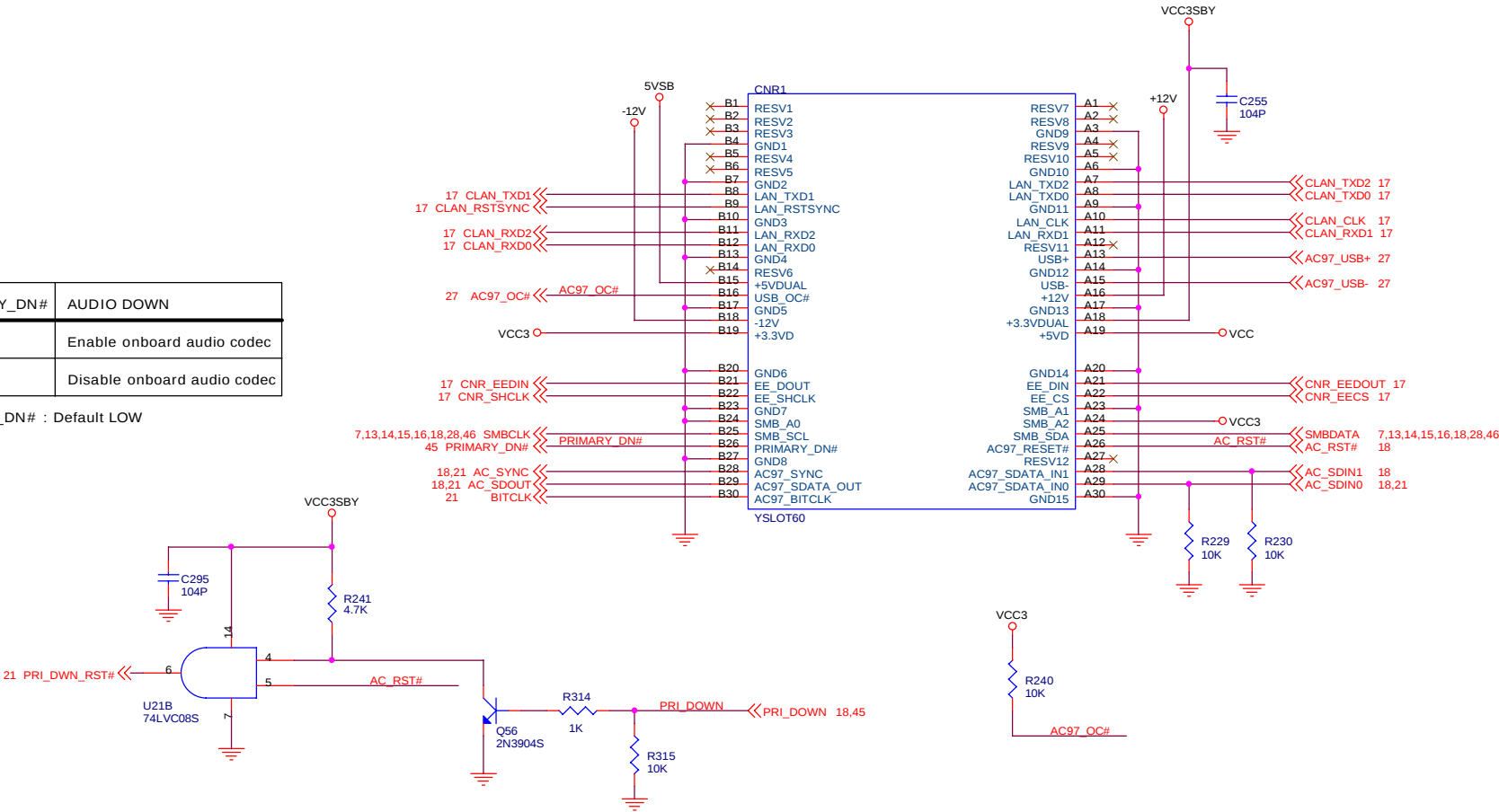
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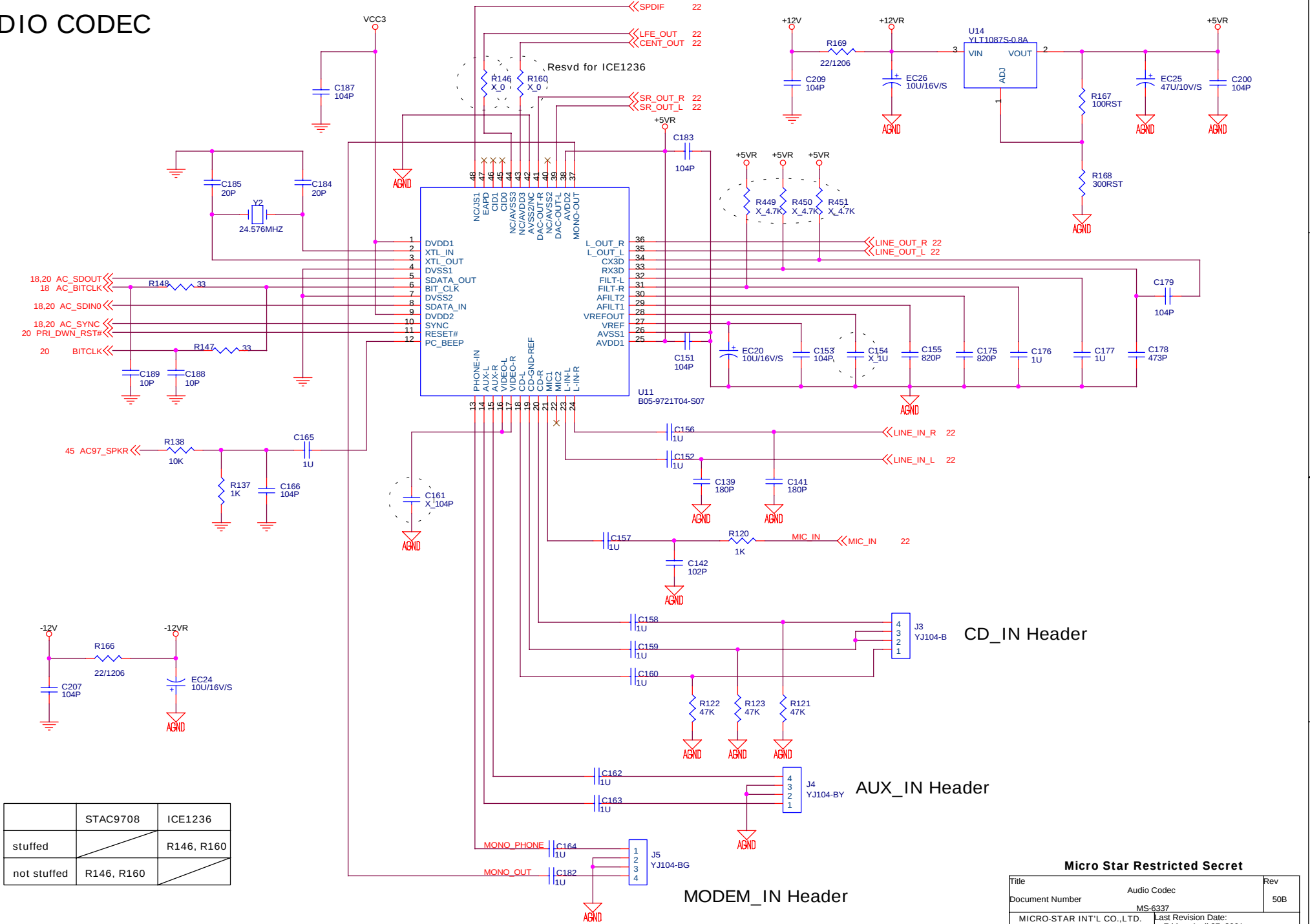
Comm. Networking Riser

PRIMARY_DN#	AUDIO DOWN
LOW	Enable onboard audio codec
HIGH	Disable onboard audio codec

PRIMARY_DN# : Default LOW



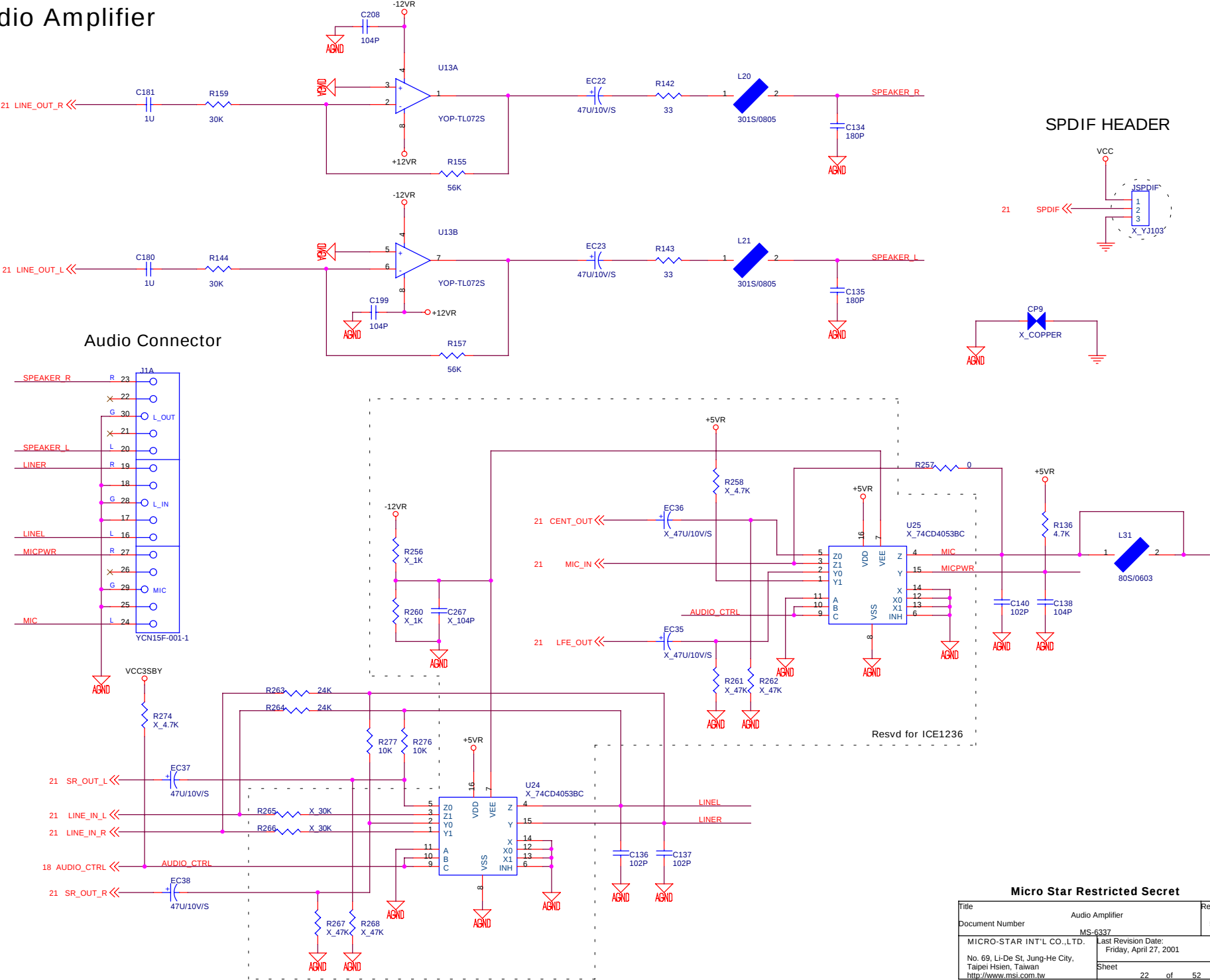
AUDIO CODEC



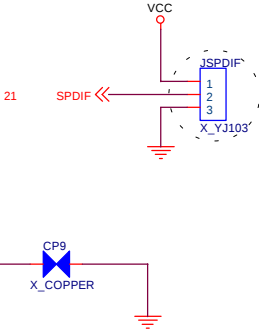
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Title	Audio Codec	Rev
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Audio Amplifier



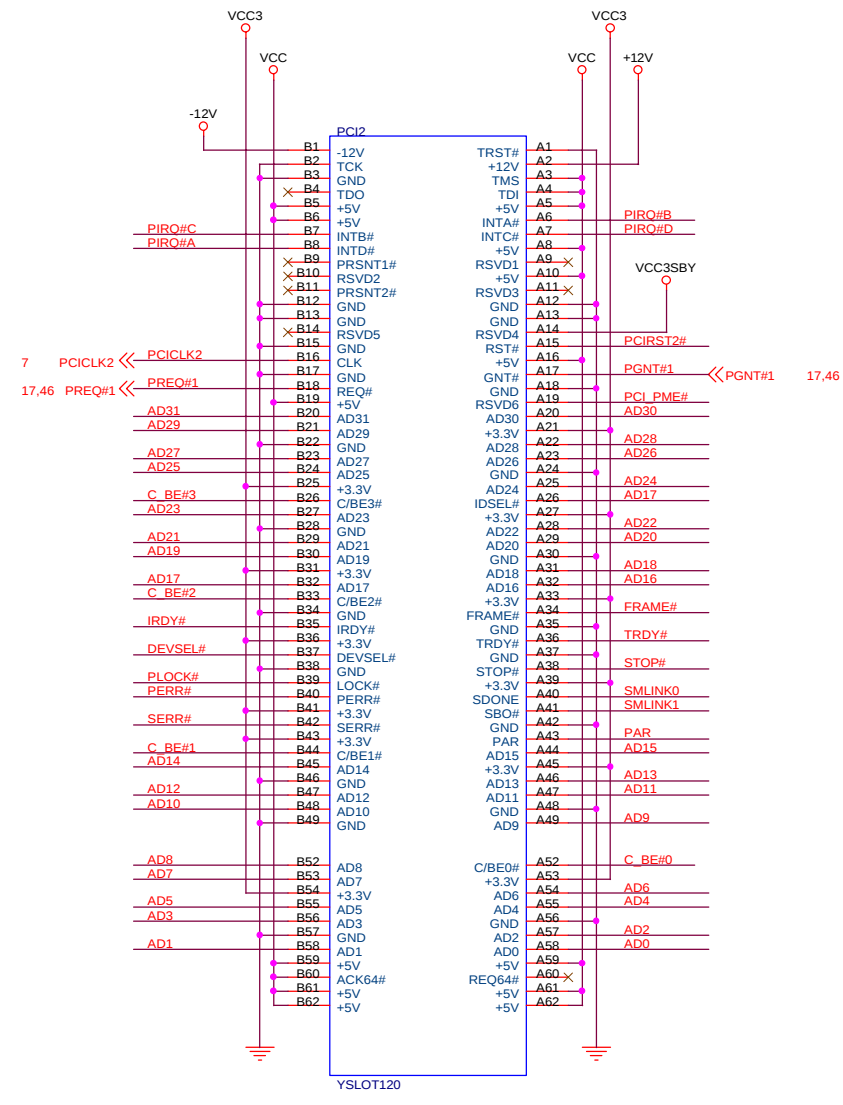
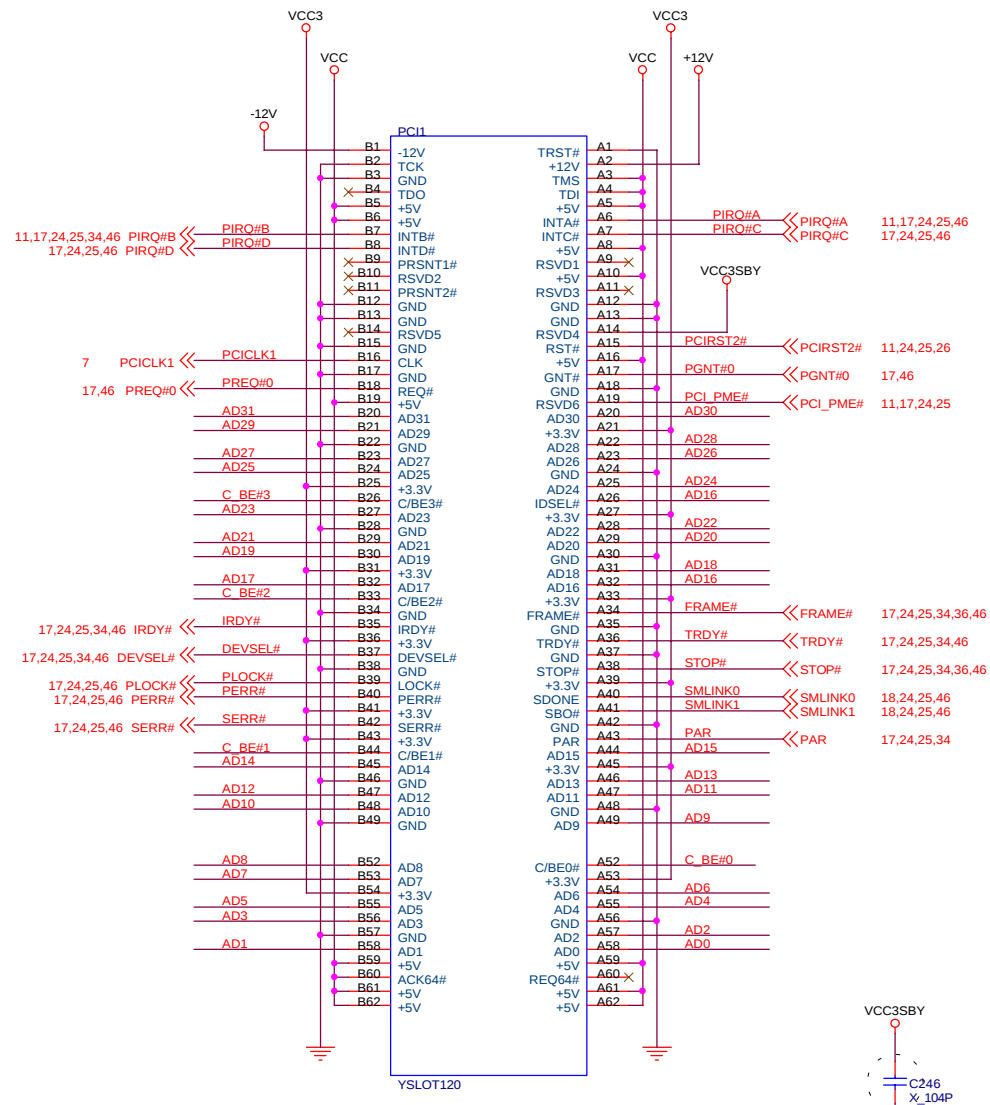
SPDIF HEADER



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PCI Connectors



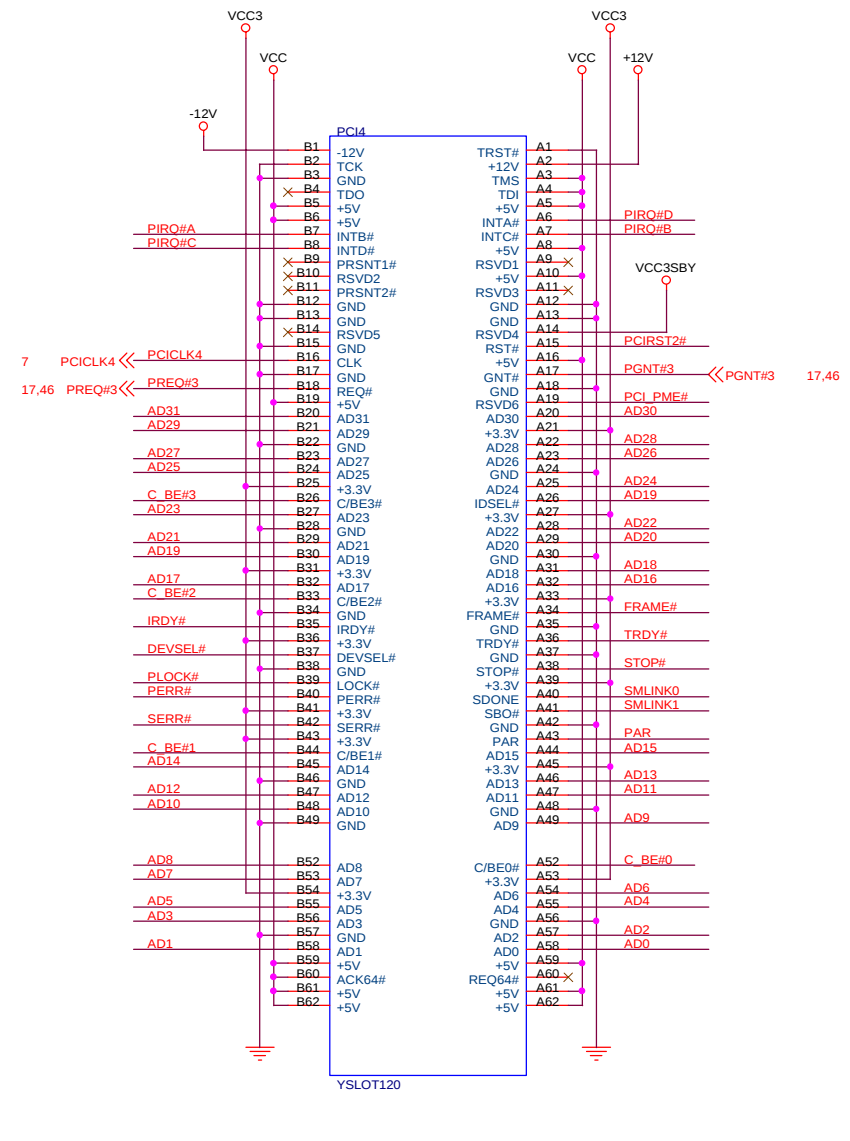
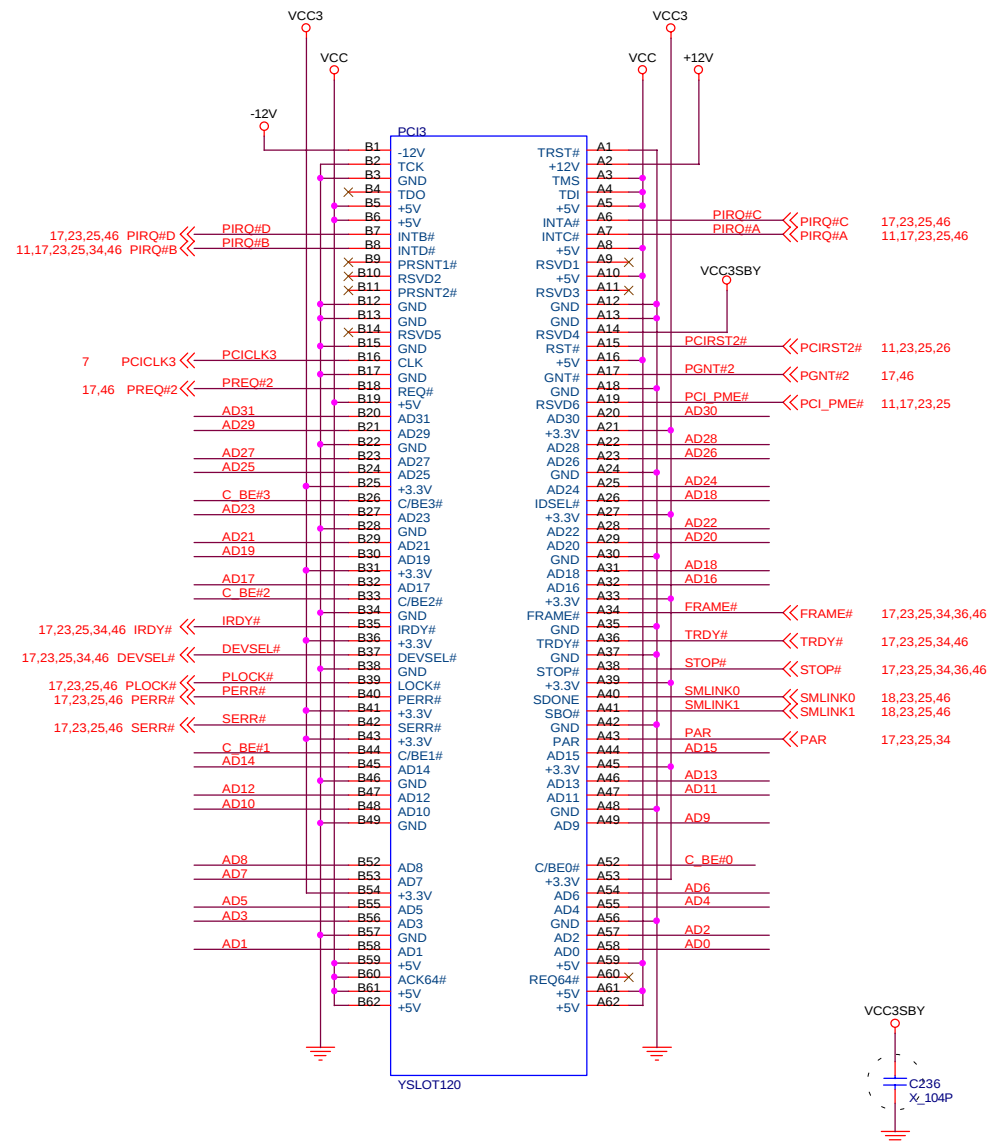
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Title	PCI Connector 1 & 2	Rev	
Document Number	MS-6337		50B
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PCI Connectors

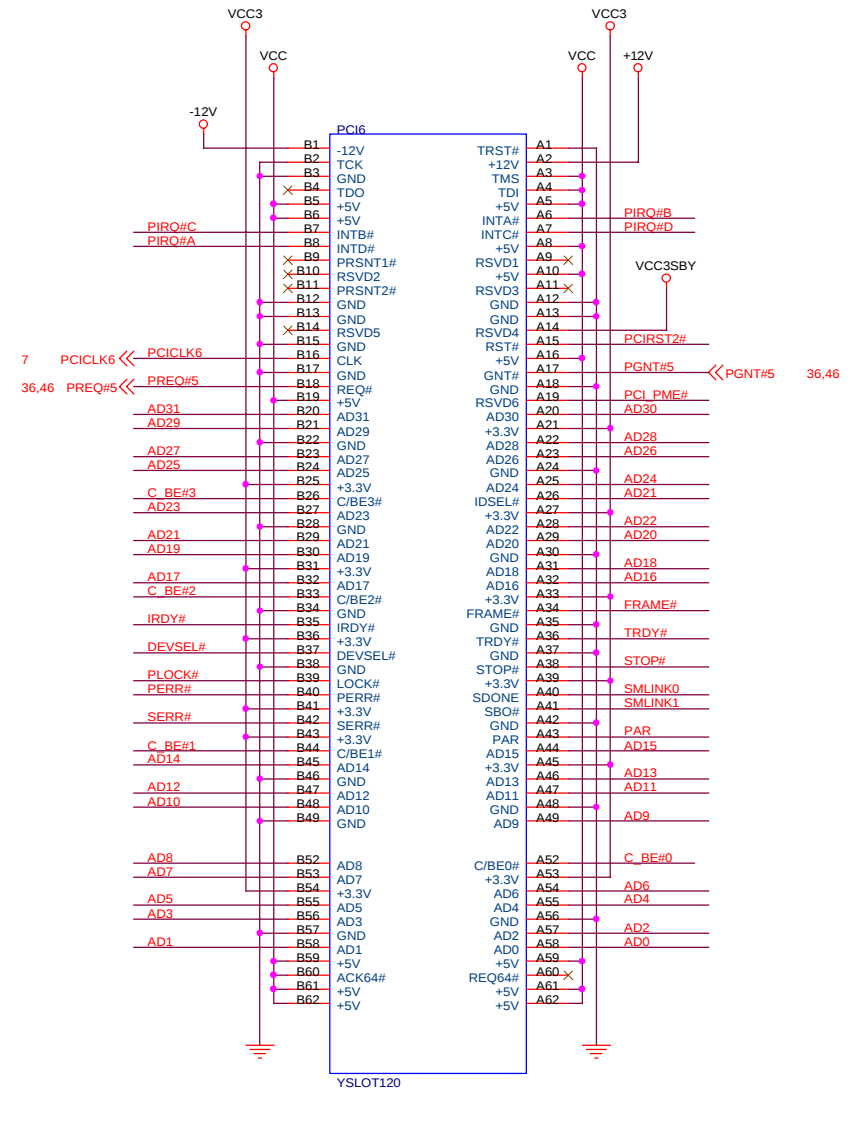
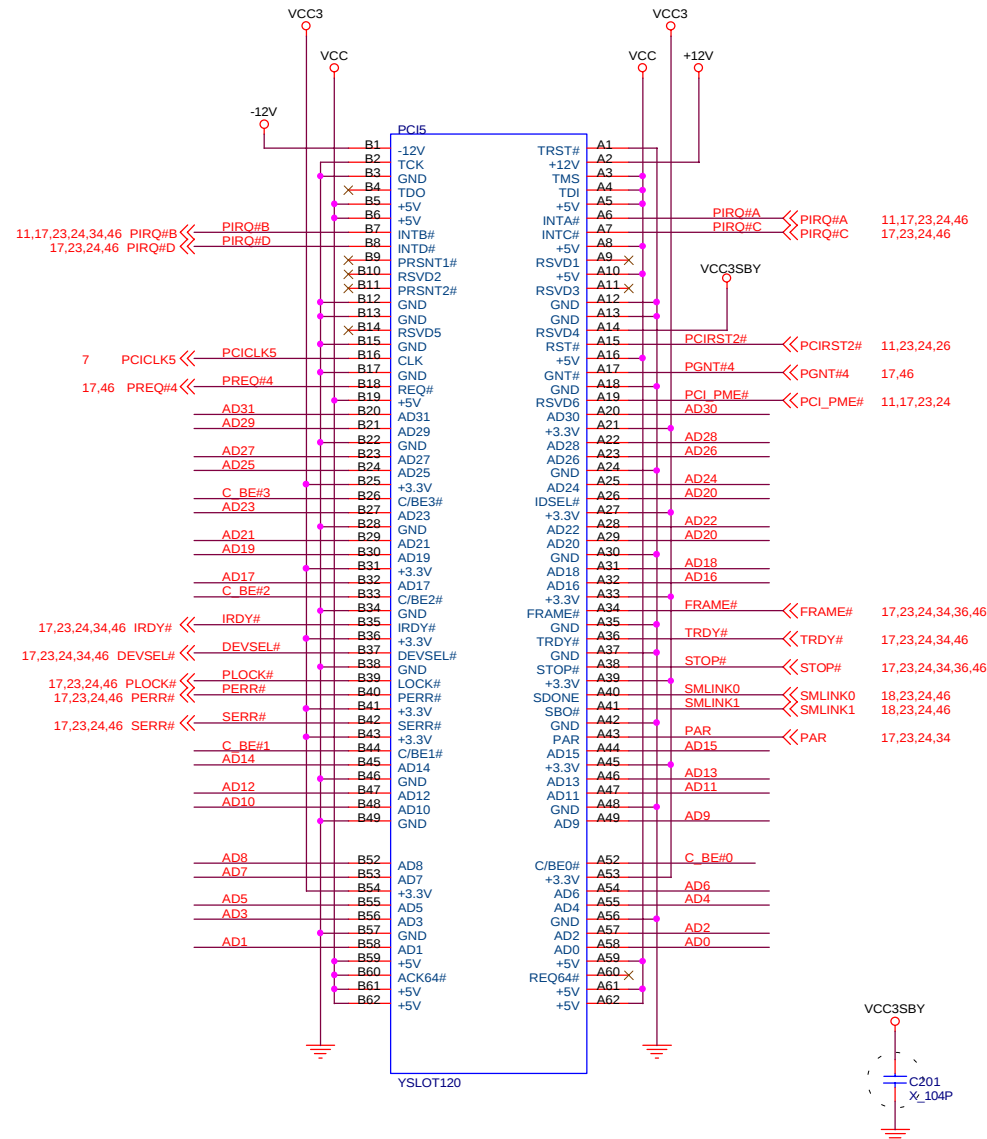


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PCI Connectors



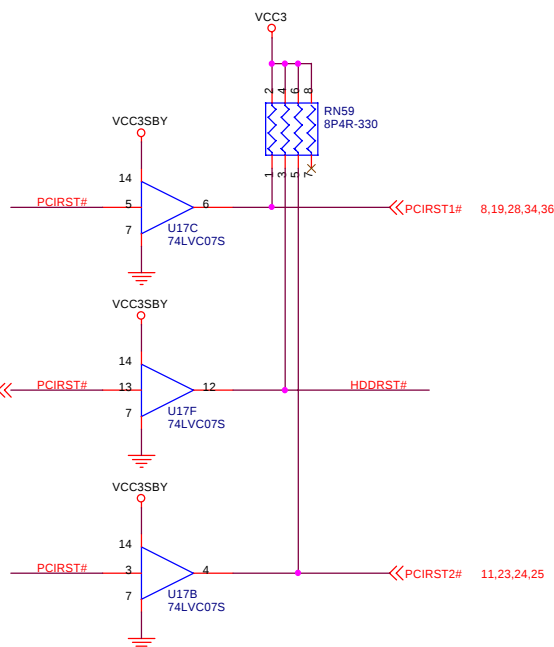
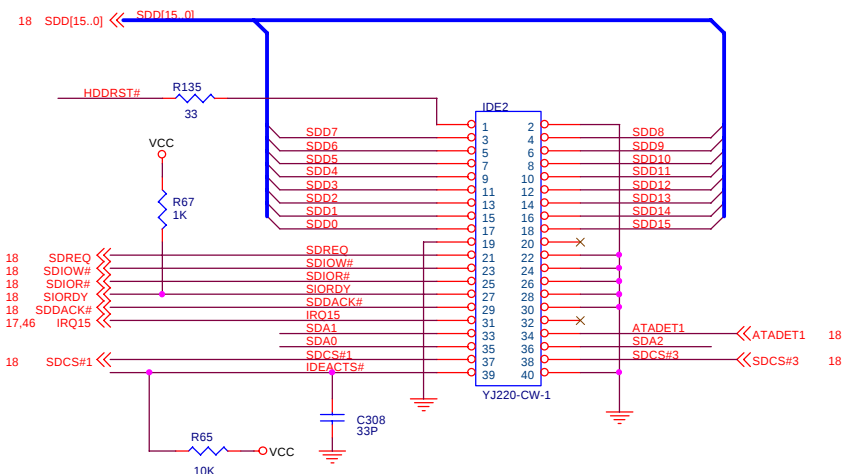
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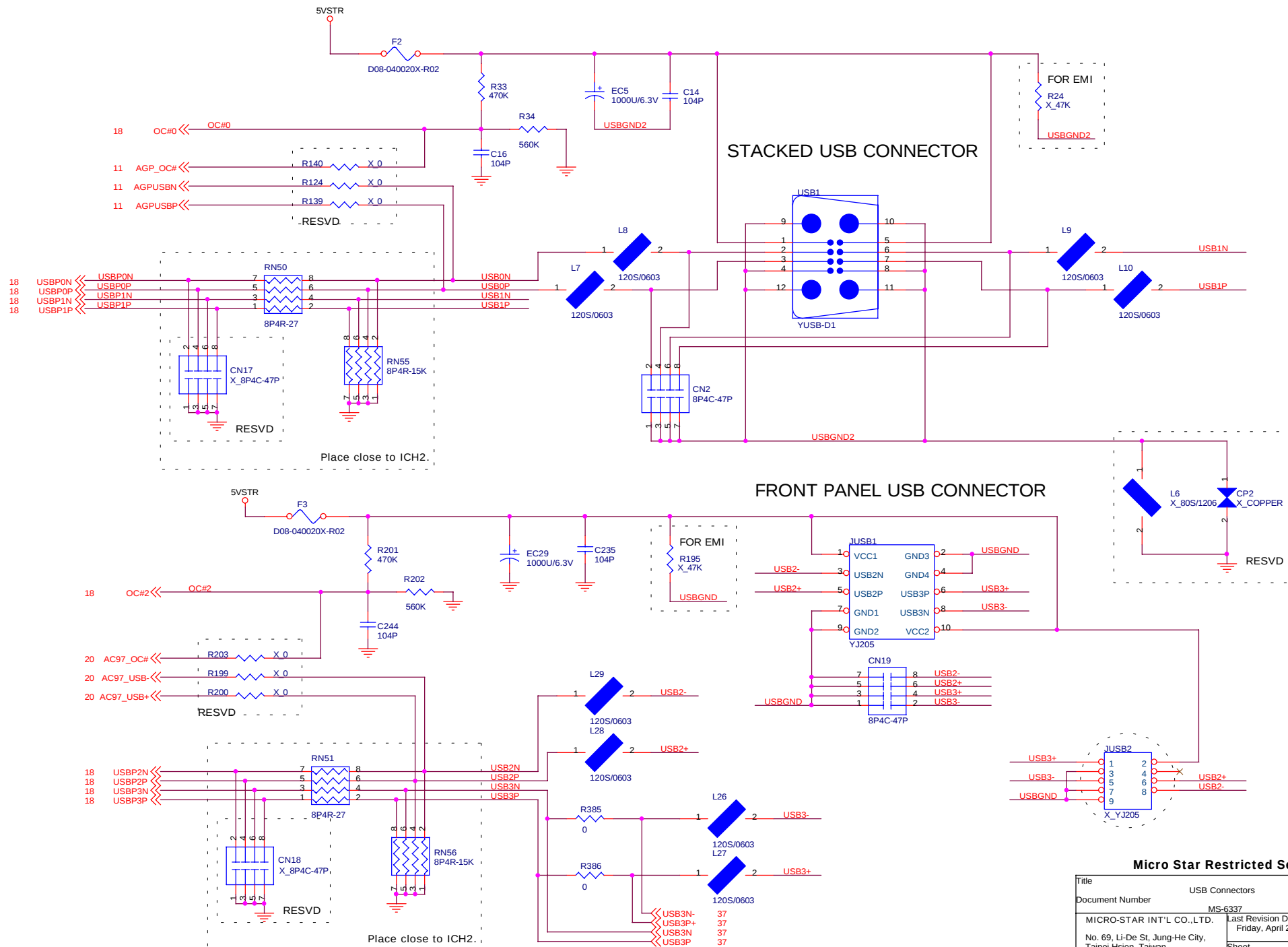
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SECONDARY IDE CONN.



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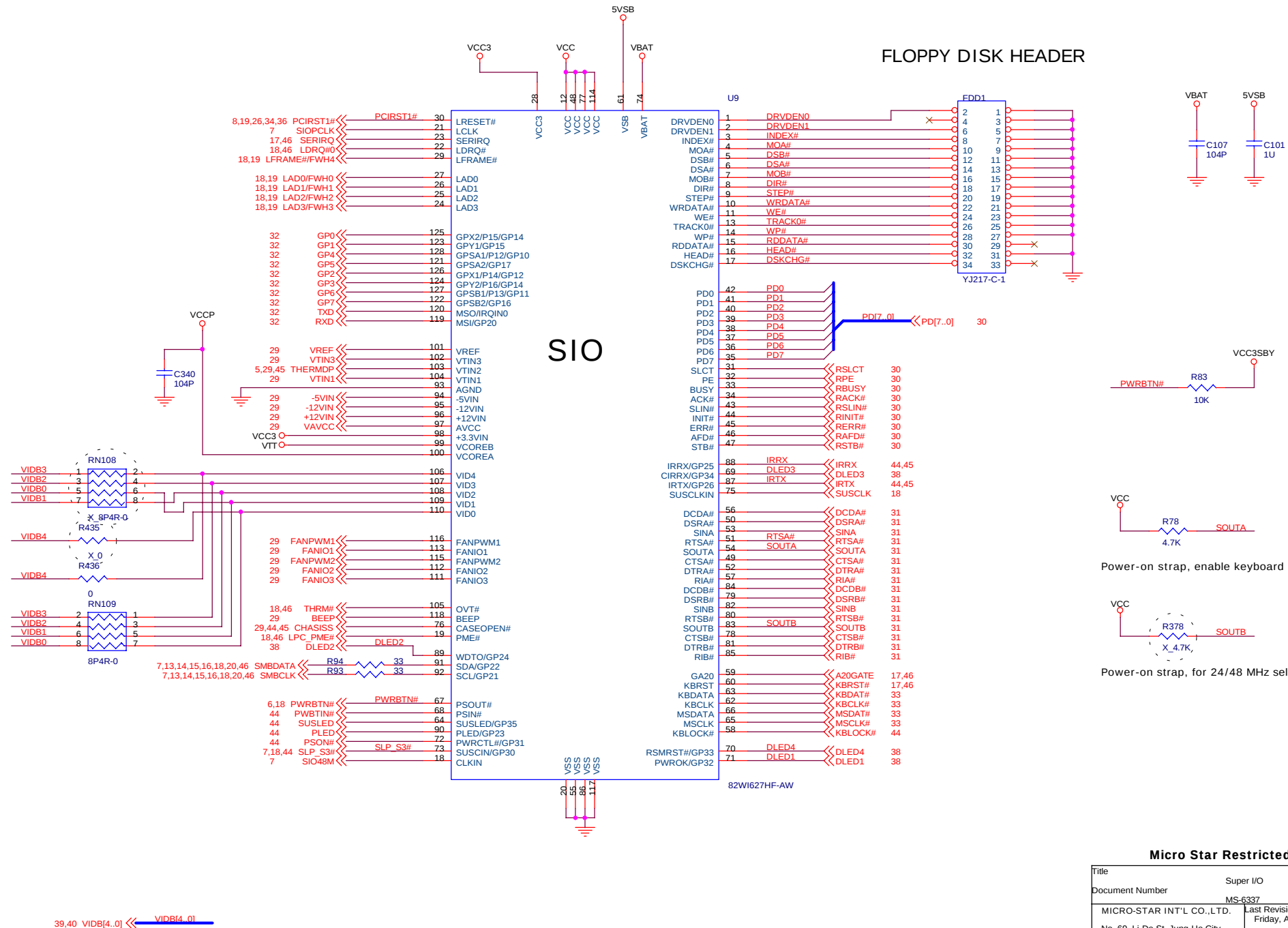
USB Connectors



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Title	USB Connectors	Rev
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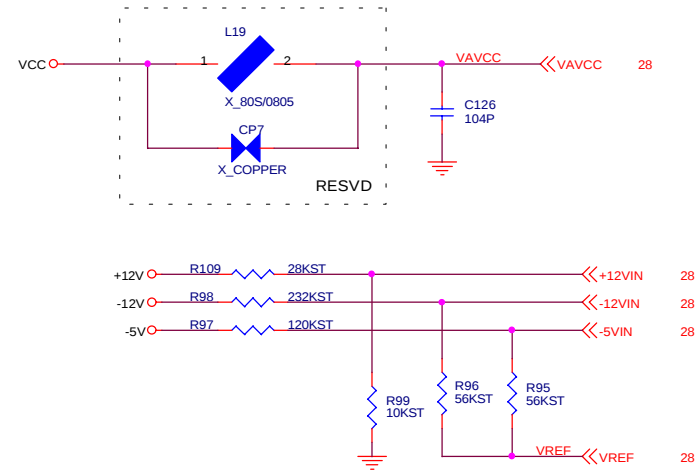
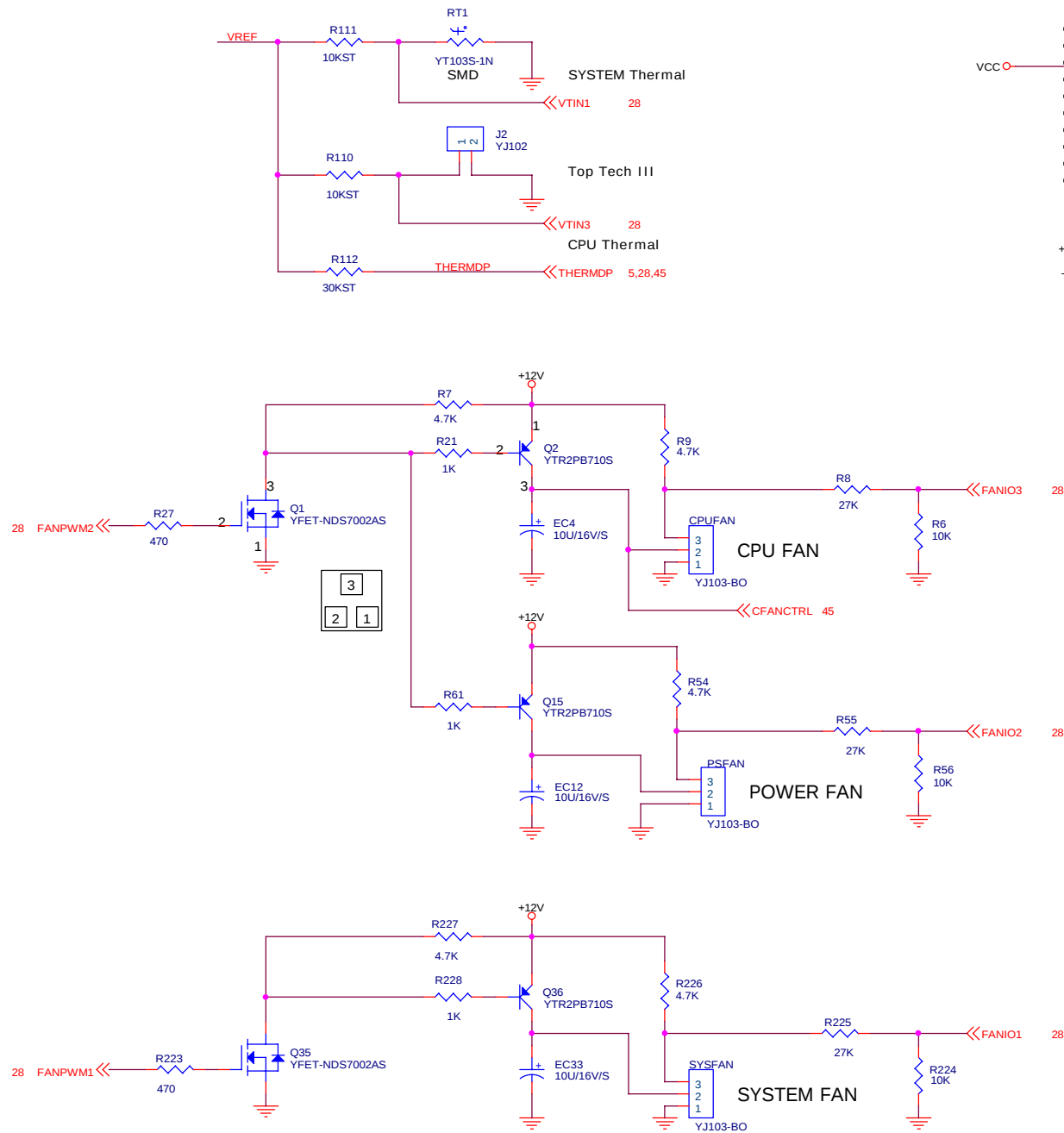
Super I/O



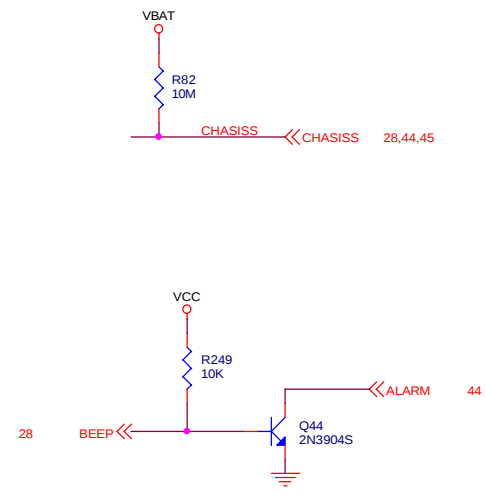
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Hardware Monitor



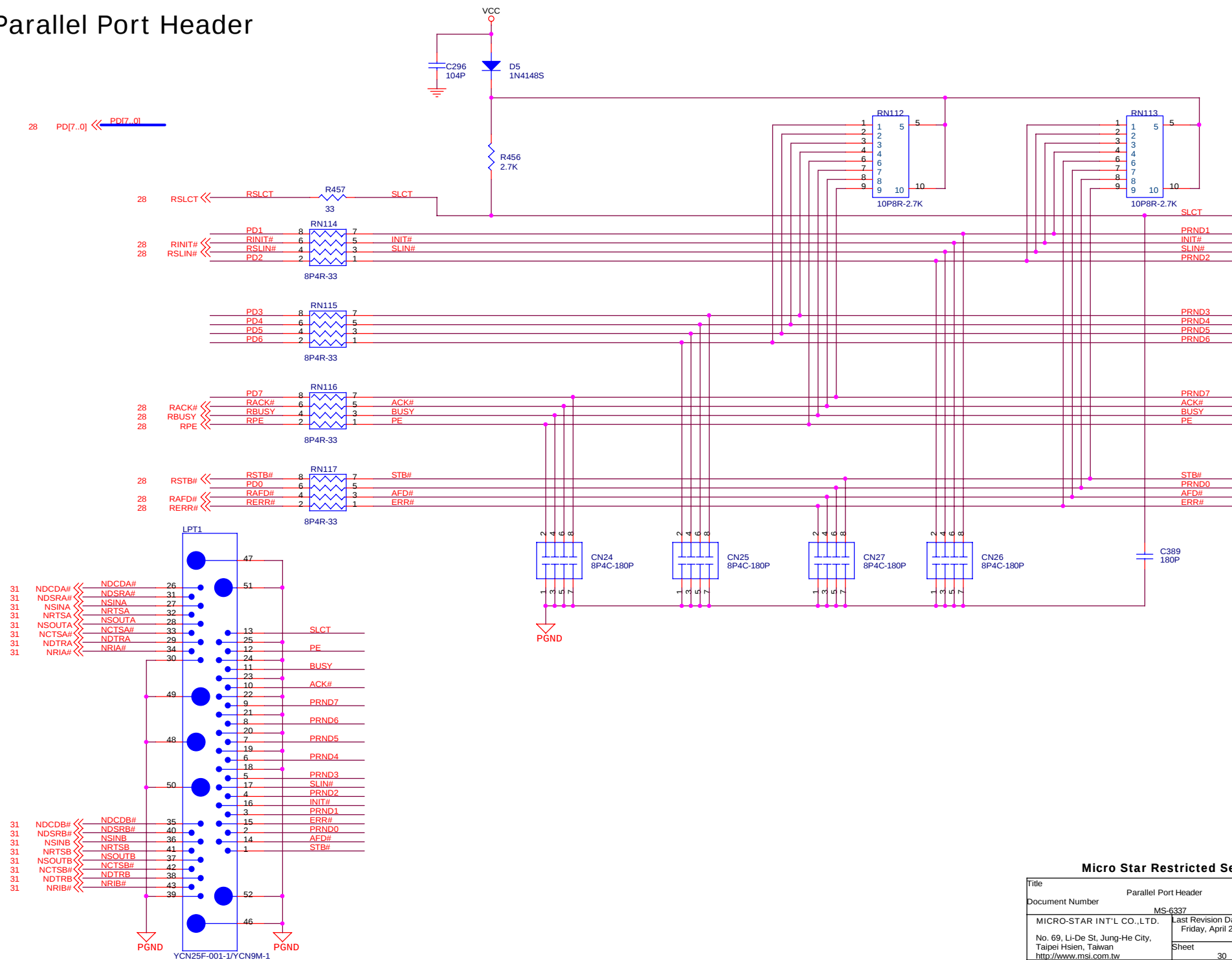
Chassis Intrusion Header



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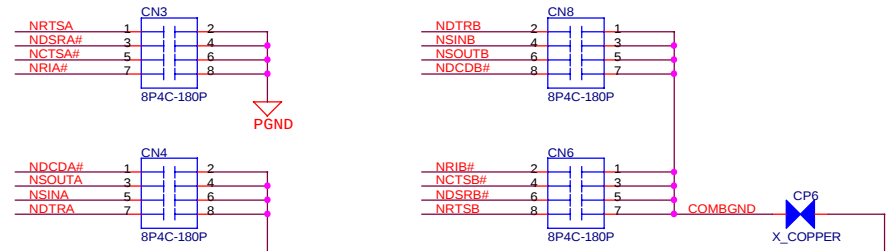
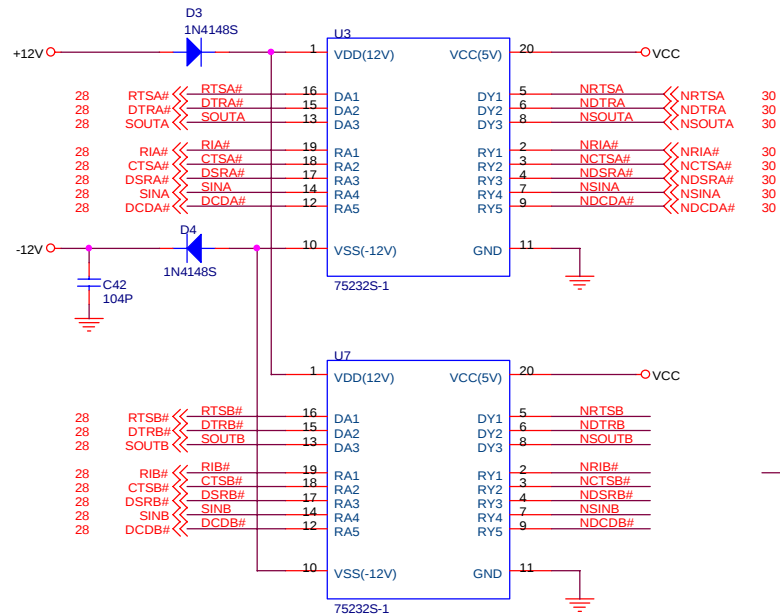
Parallel Port Header



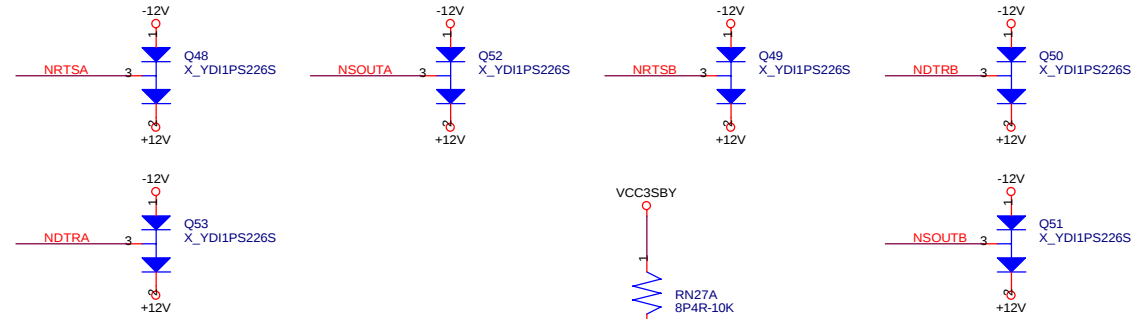
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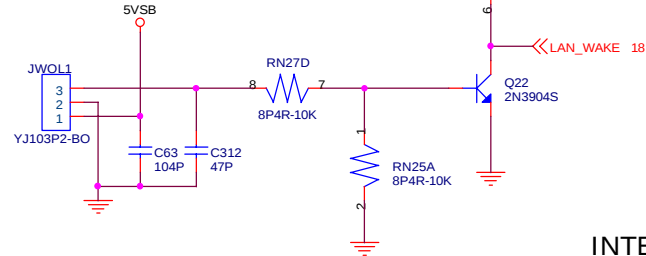
Serial Port/COM Headers



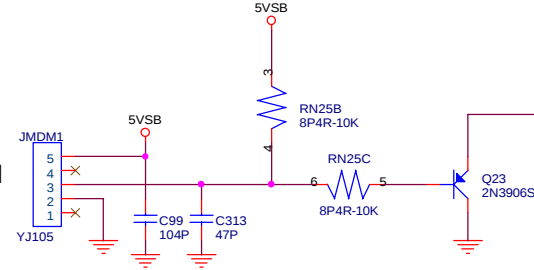
COM2 HEADER



LAN WAKEUP HEADER



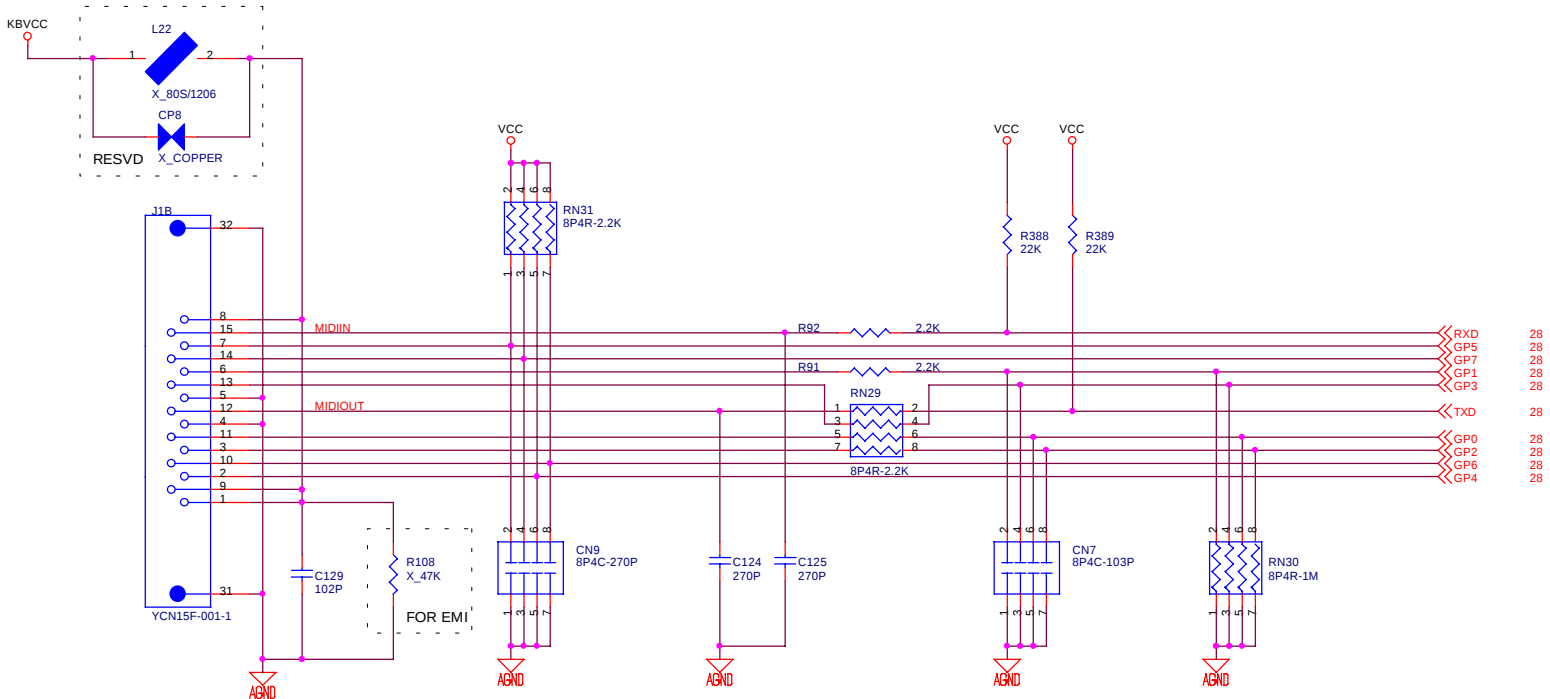
INTERNAL MODEM WAKEUP HEADER



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Title	Serial Port Header	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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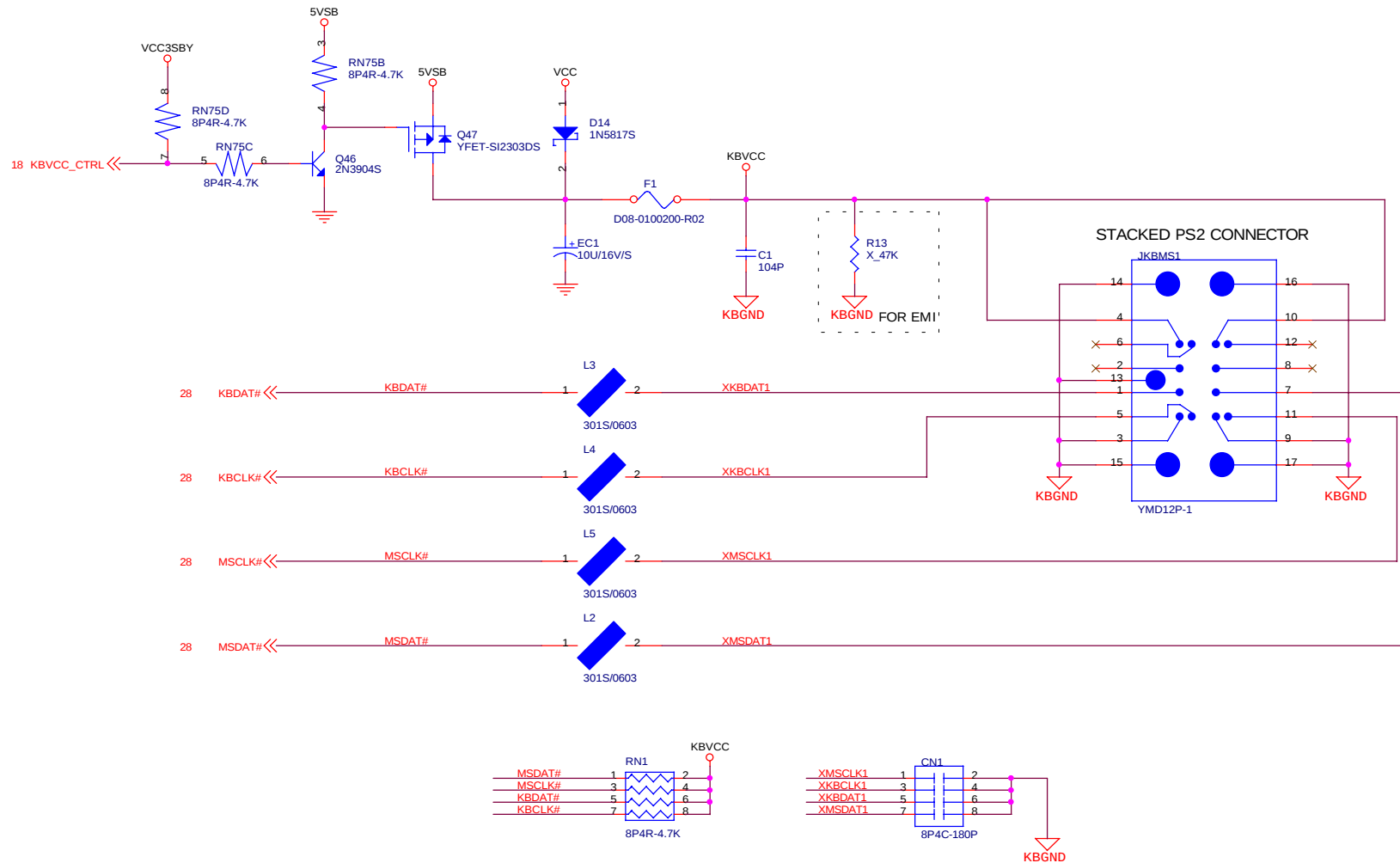
Game Port



GAME PORT HEADER

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Title	Game Port Header	Rev
Document Number	MS-6337	50B
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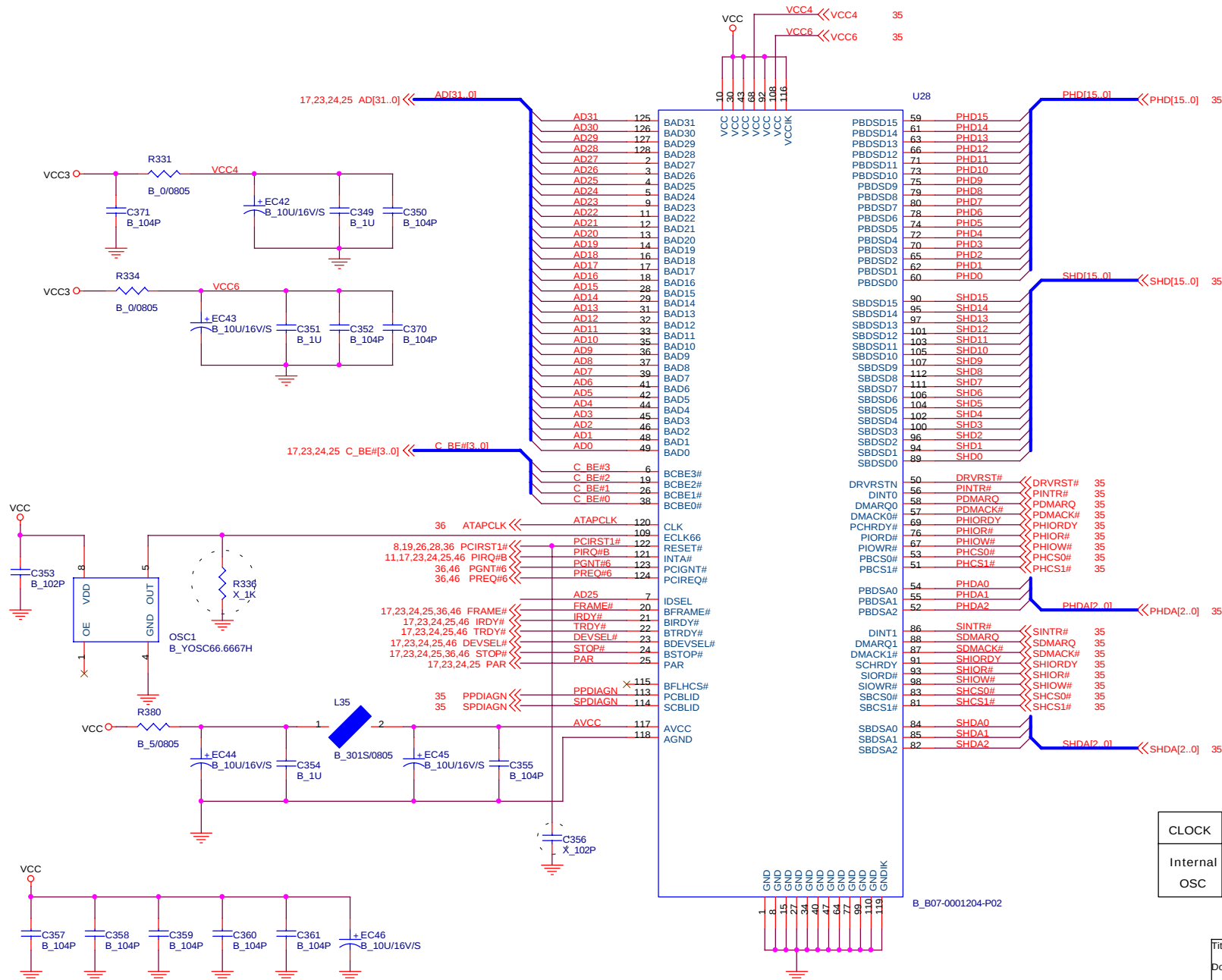
Keyboard/Mouse Ports



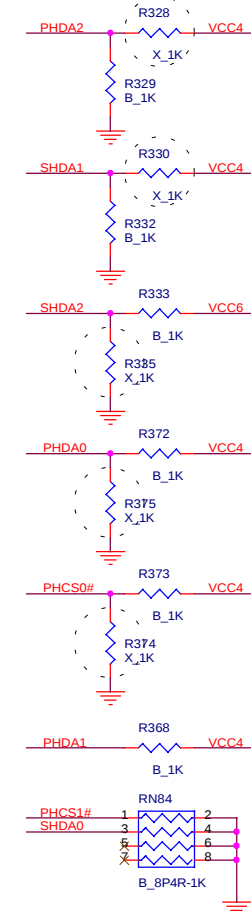
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Title	Keyboard/Mouse Ports	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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PCI Utra 100 Controller



RESET STRAPS



Function	PHDA2	PHCS1#
IDE	1	0
Raid	0	0

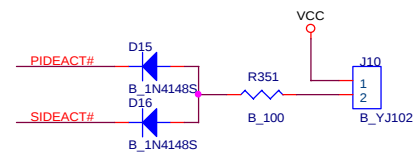
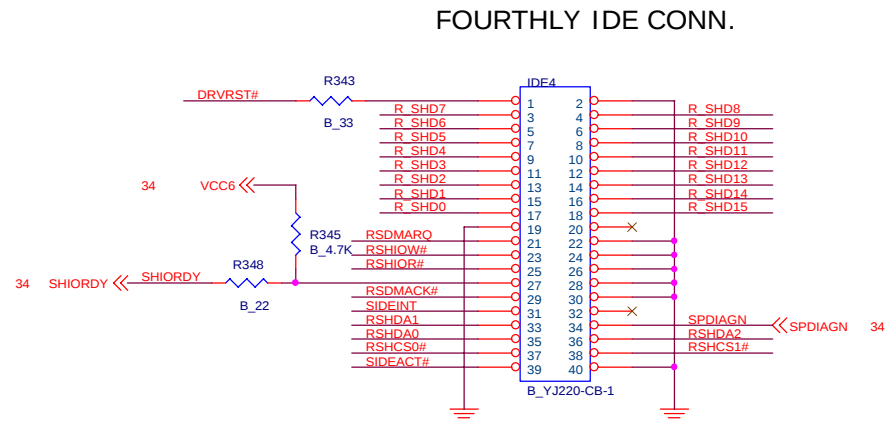
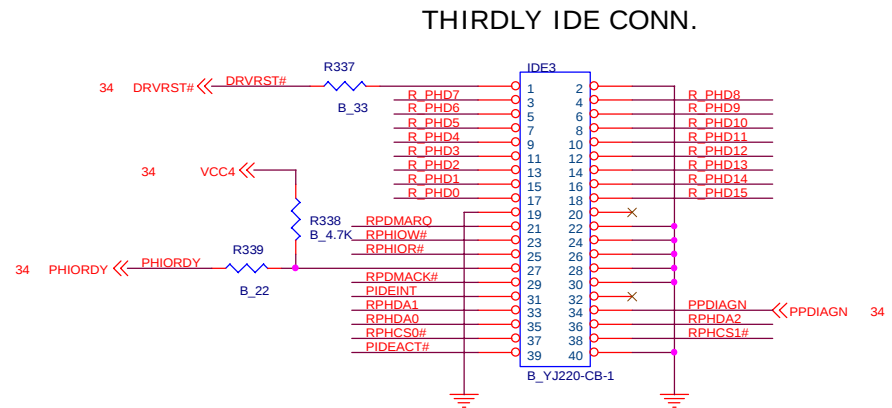
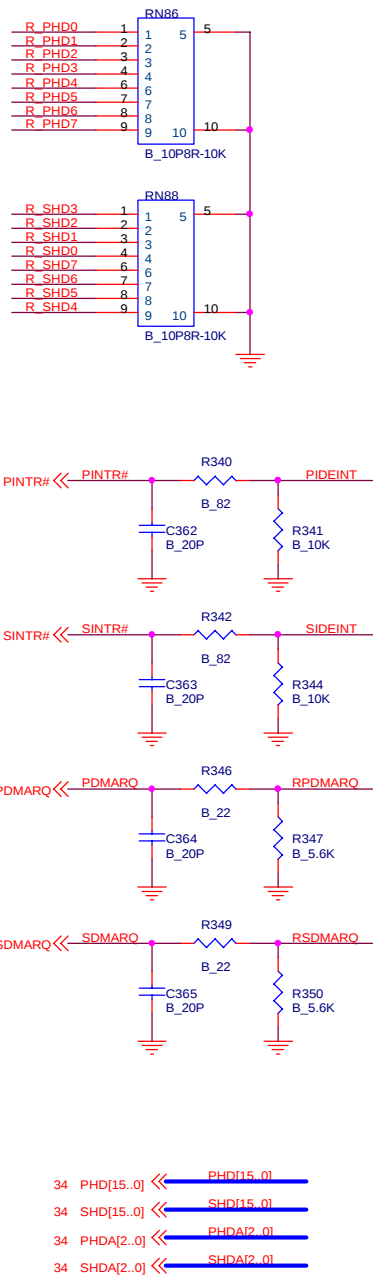
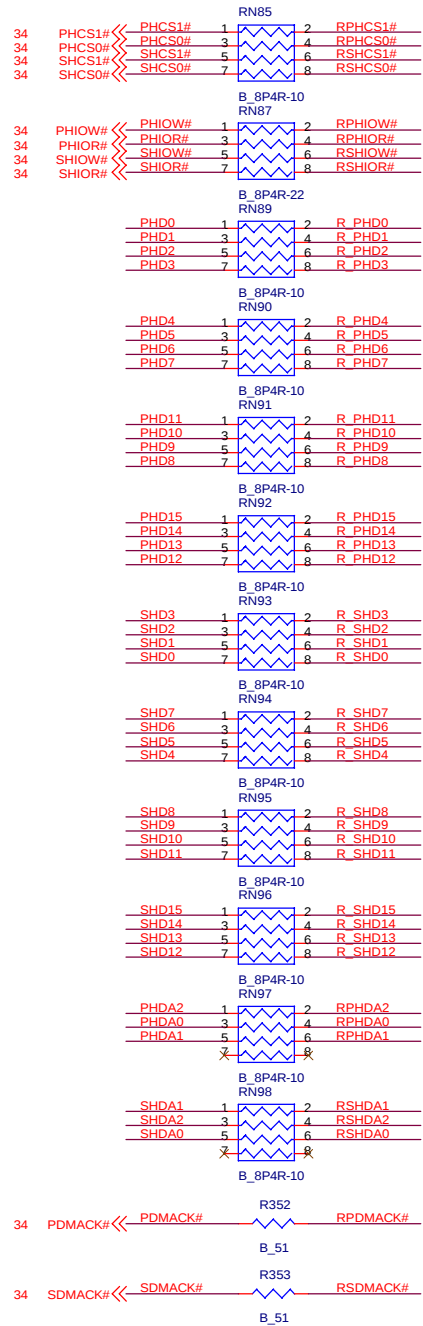
CLOCK	SHDA
Internal	0
OSC	1

BIOS Size	PHCS1#	SHDA1
64K	0	0
128K	1	X

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Title	PCI Ultra 100 Controller	Rev	
Document Number	MS-6337		50B
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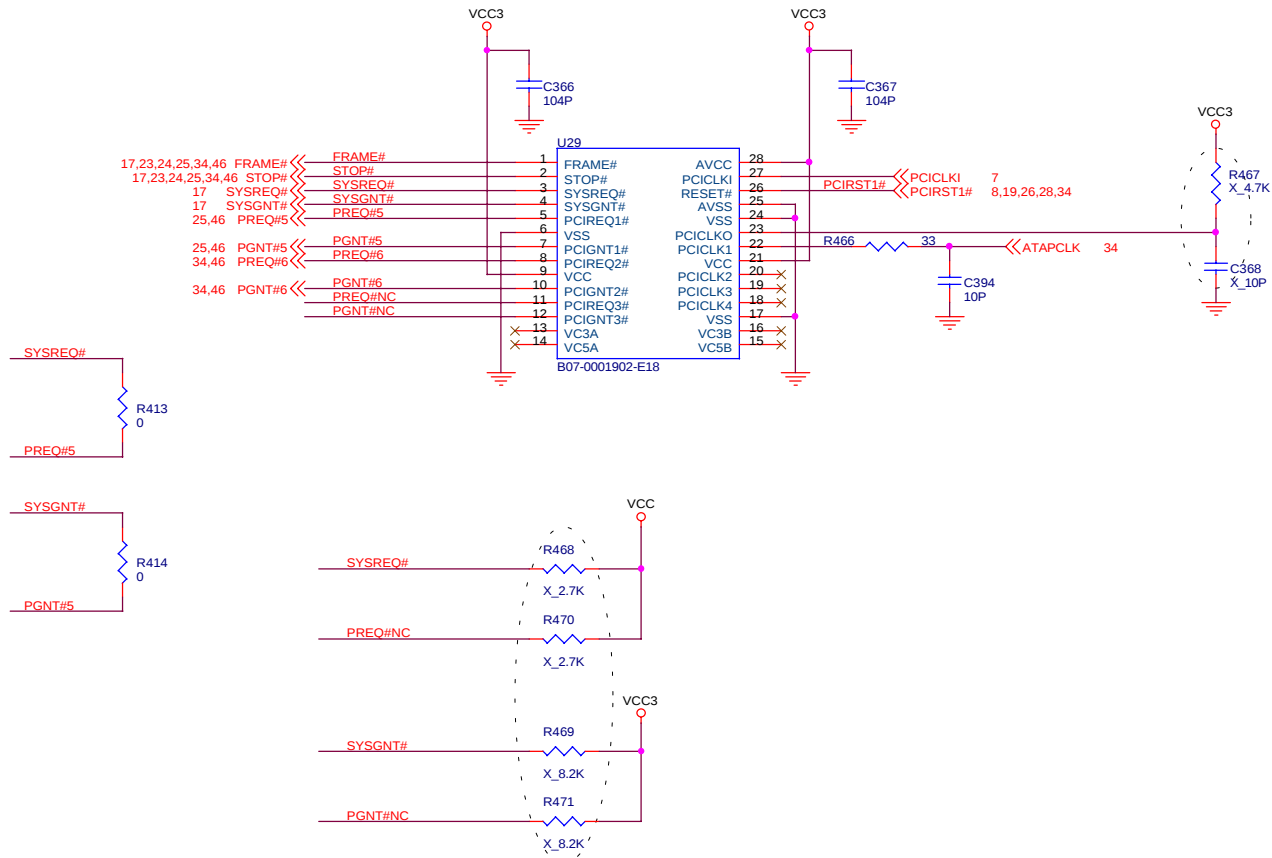
PCI Ultra 100 Connectors



Micro Star Restricted Secret

Title	Ultra 100 Connectors	Rev	
Document Number	MS-6337		50B
MICRO-STAR INT'L CO.,LTD.	Last Revision Date:		
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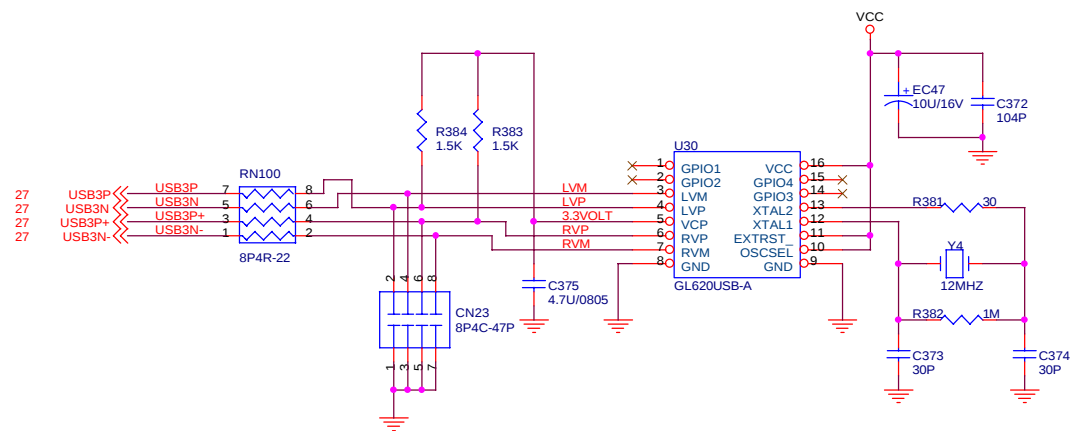
PLL and PCI Arbitor



Micro Star Restricted Secret

Title	PLL and PCI Arbiter	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.	Last Revision Date:	
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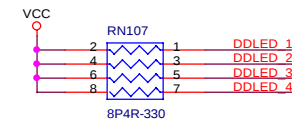
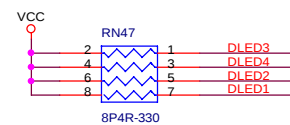
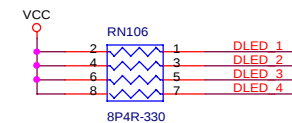
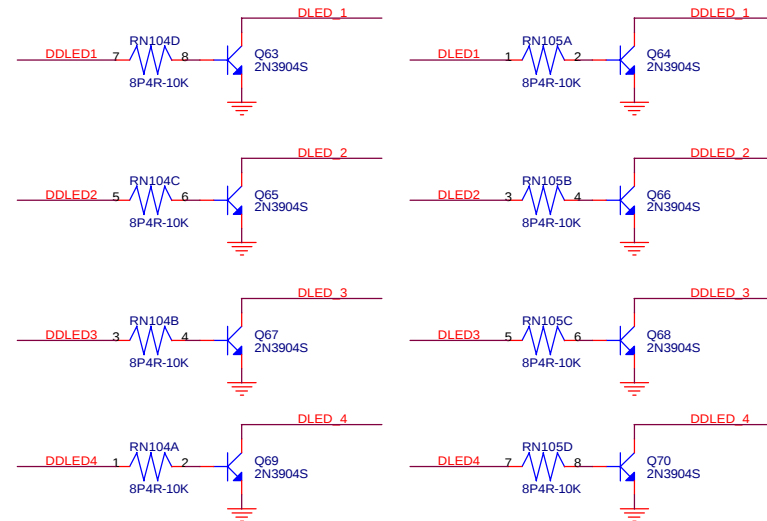
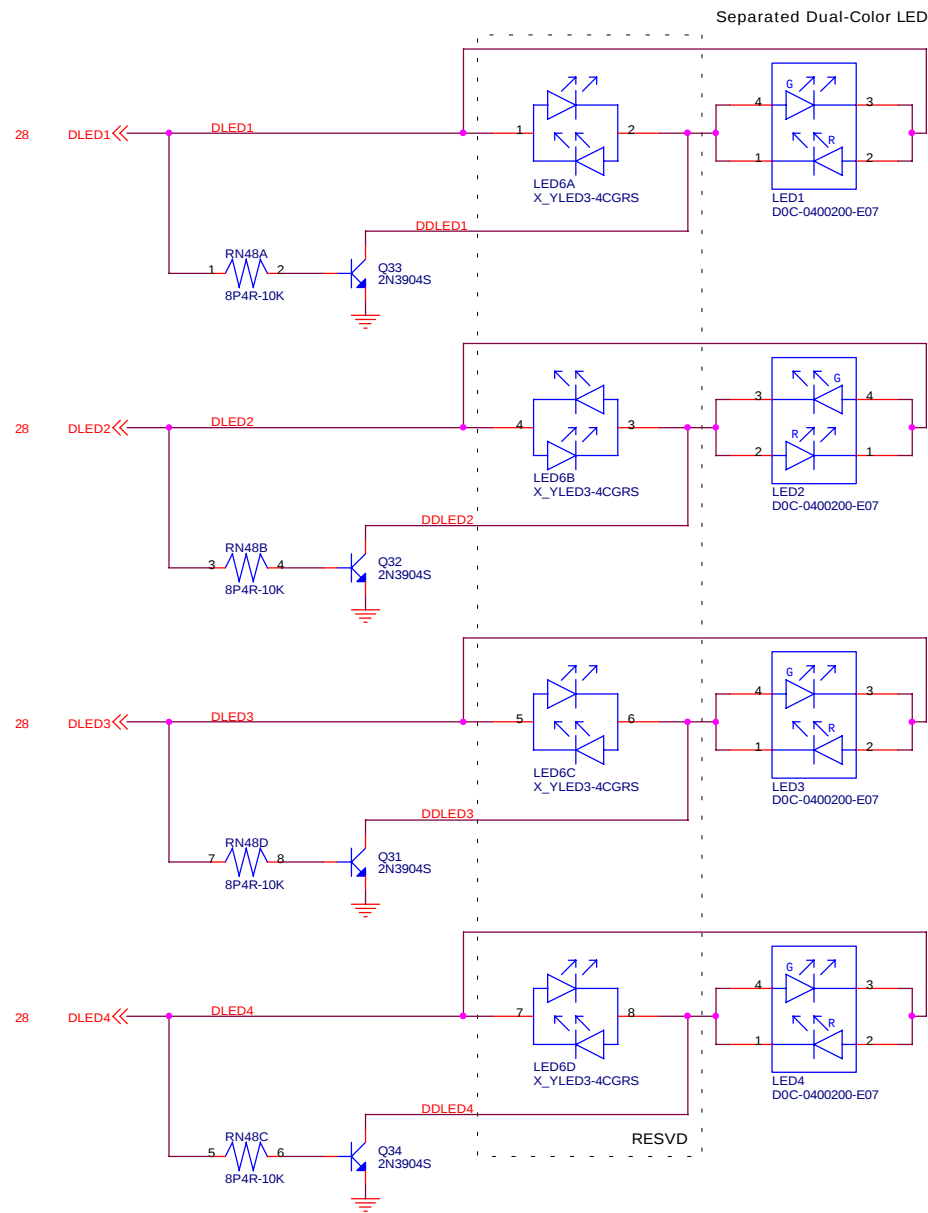
PC to PC Networking Controller



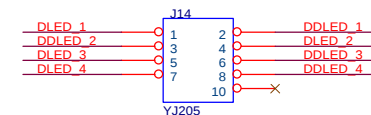
Micro Star Restricted Secret

Title	PC to PC Networking Controller	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Smart Diagnostic LED



Smart DLED Header

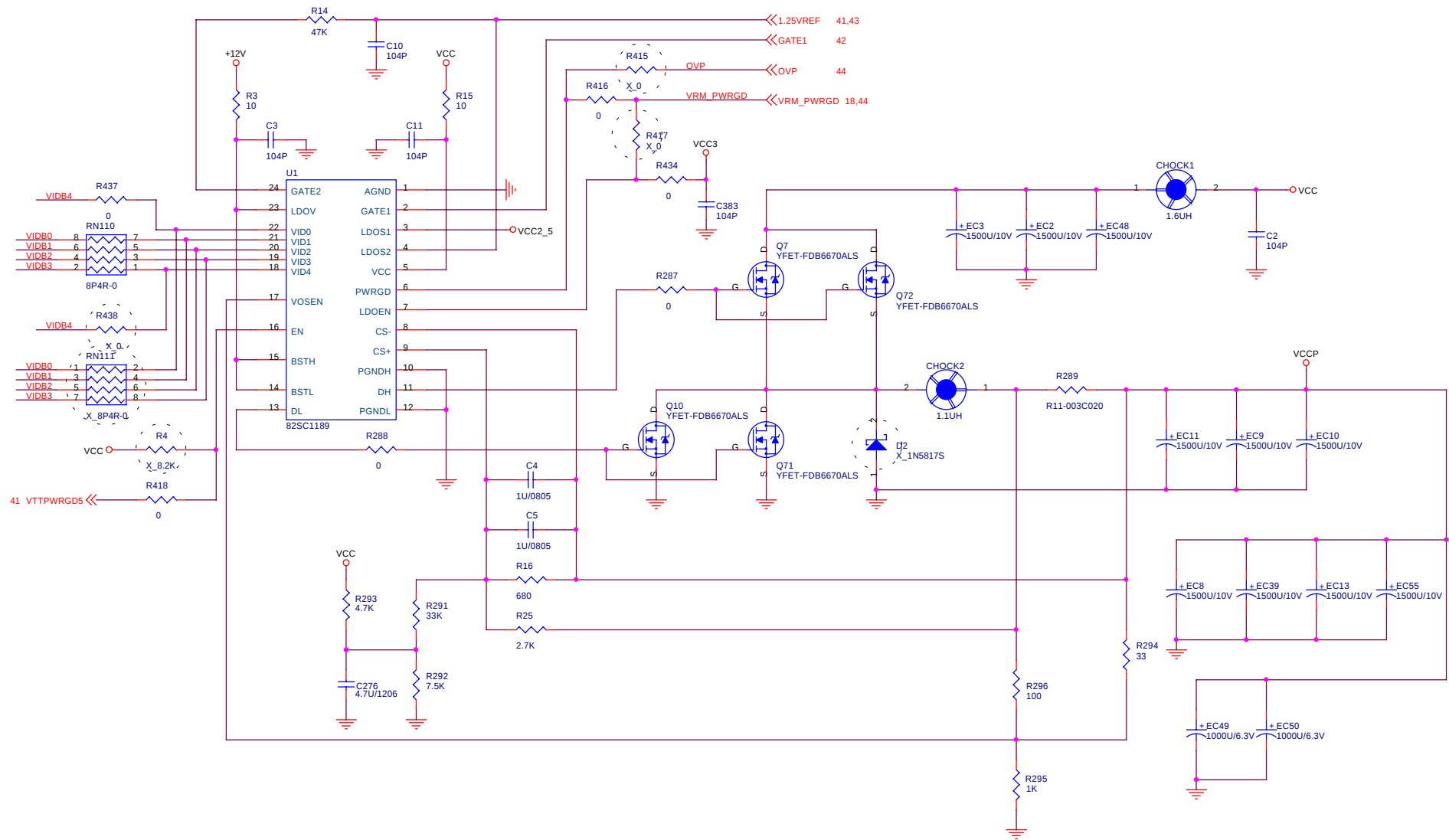


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Title	Smart Diagnostic LED	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Friday, April 27, 2001	
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VRM 8.5

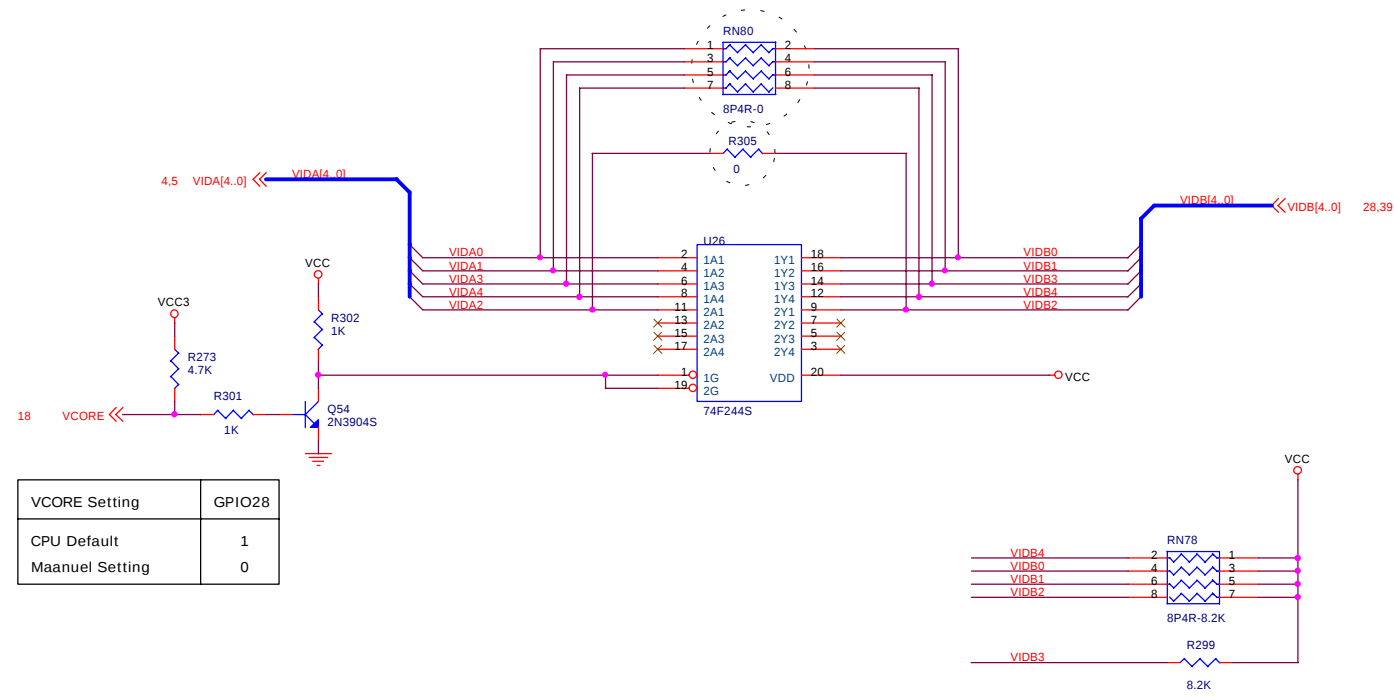
28,40 VIDB[4..0] << VIDB[4..0]



Micro Star Restricted Secret

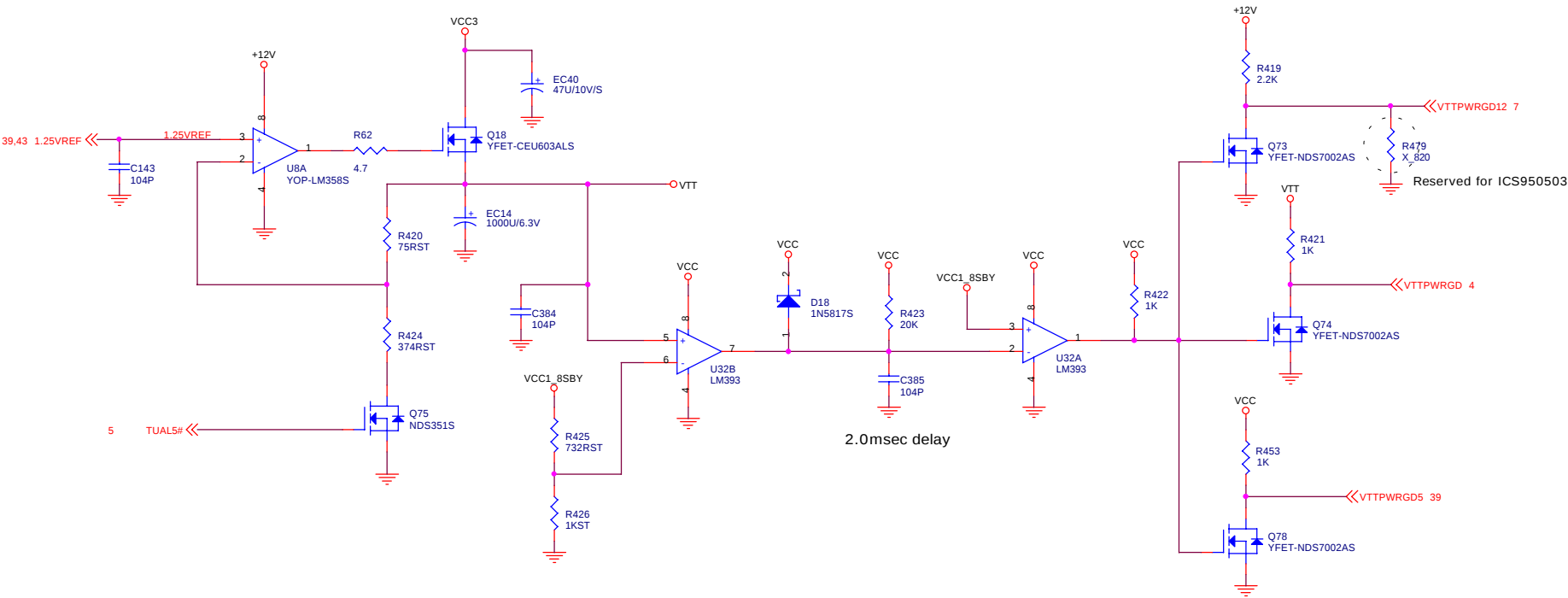
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Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Vcore Setting



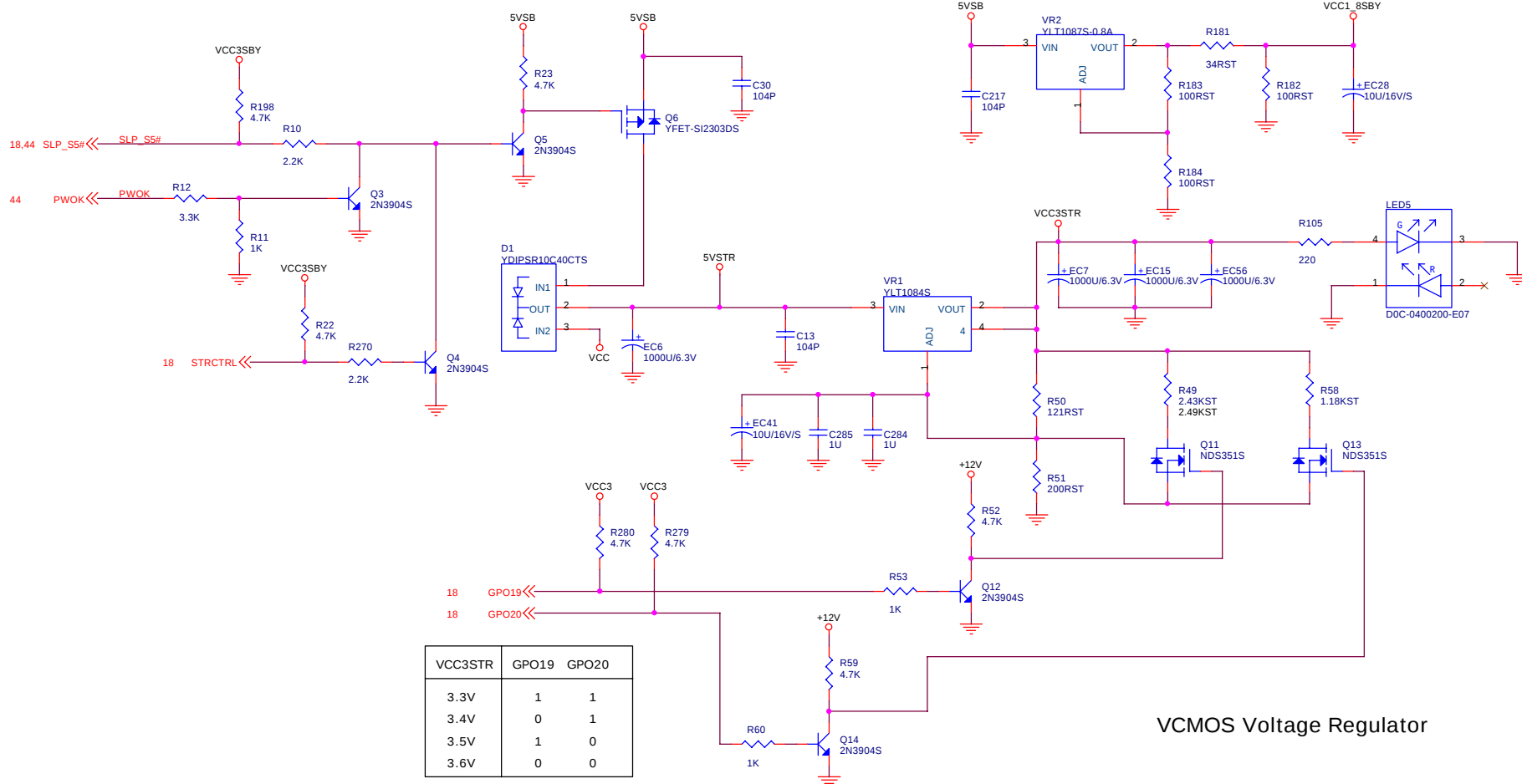
Vcore Setting	GPIO28
CPU Default	1
Maanuel Setting	0

VTT Voltage Regulators



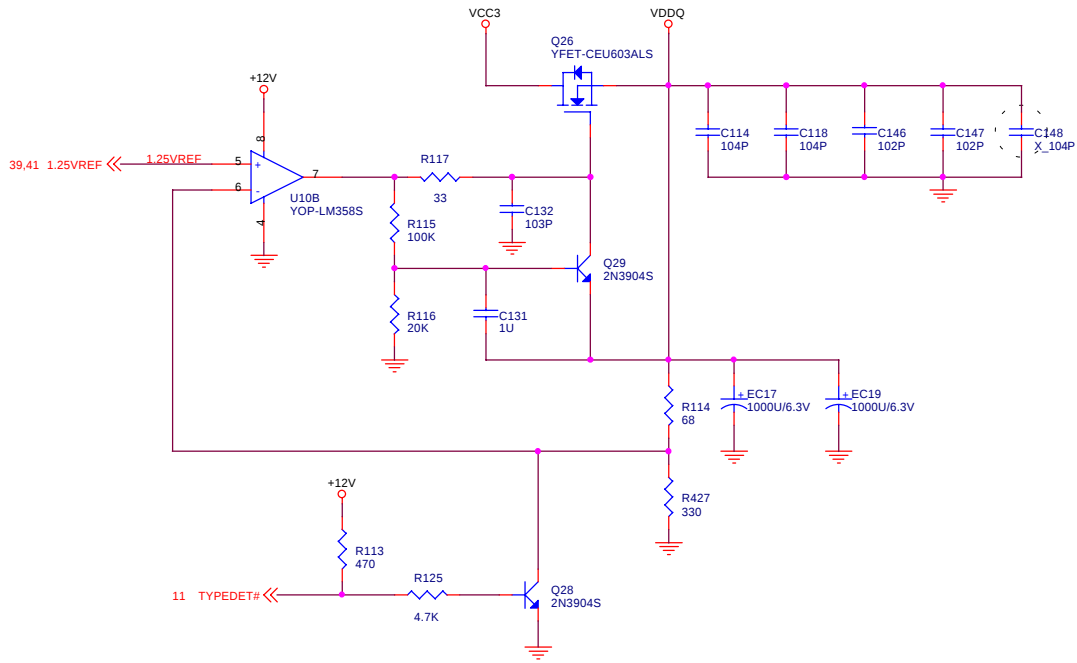
Micro Star Restricted Secret		
Title	VTT Voltage Regulators	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Voltage Regulators

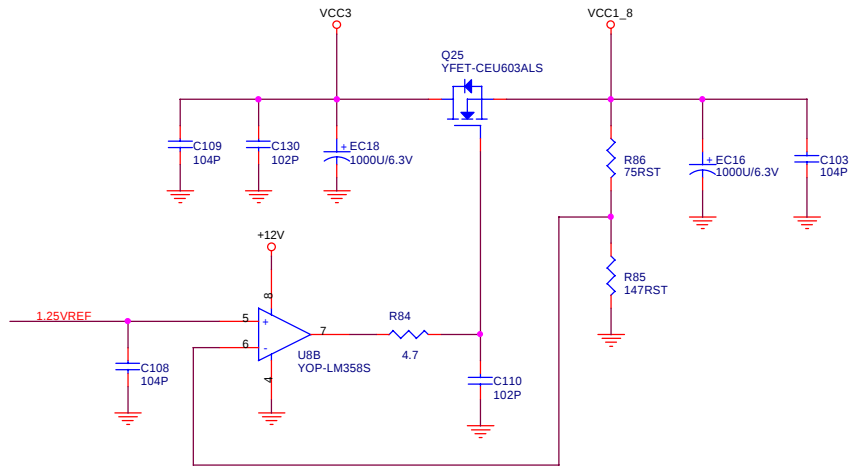


VCC3STR	GPO19	GPO20
3.3V	1	1
3.4V	0	1
3.5V	1	0
3.6V	0	0

AGP Voltage Regulators



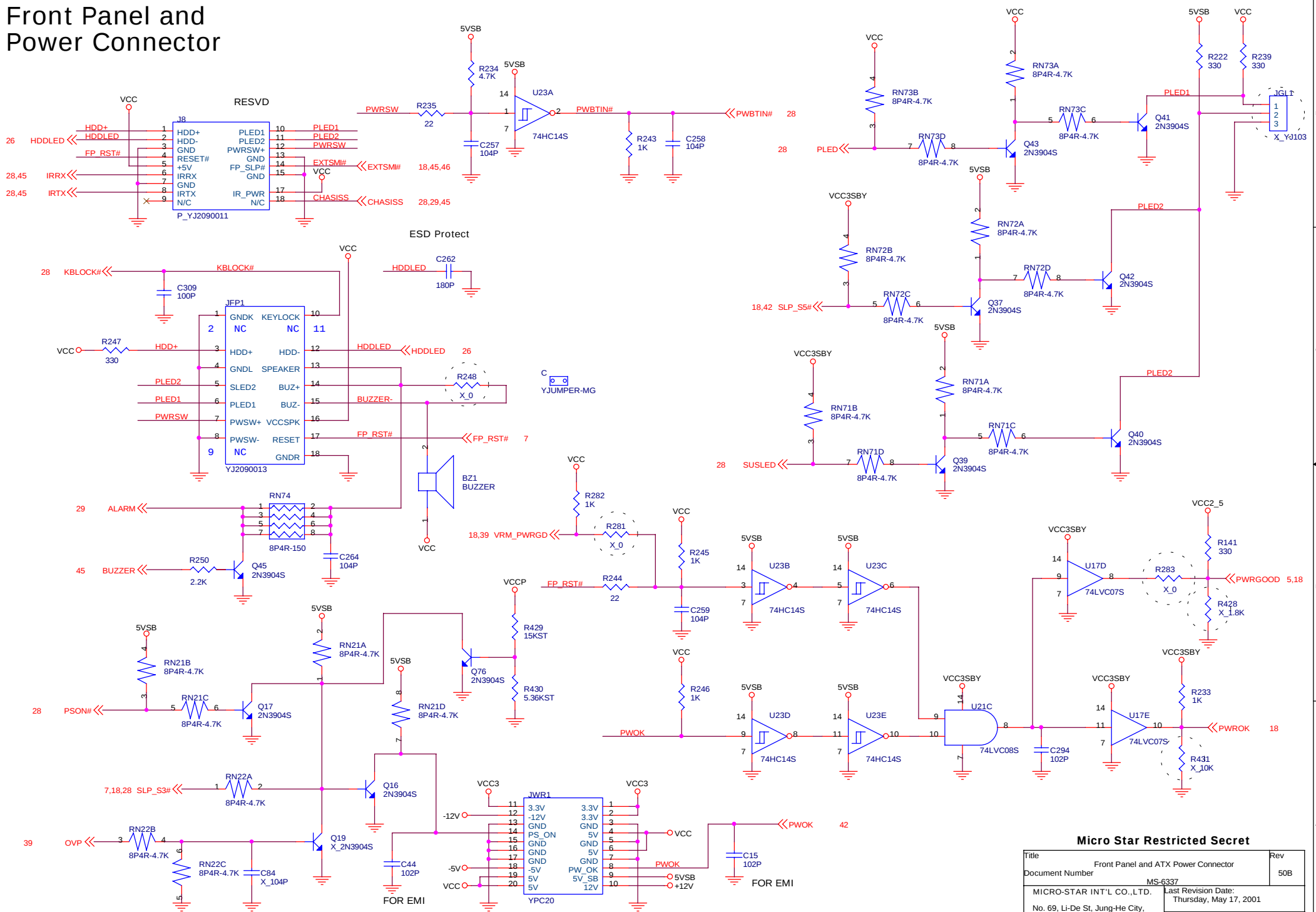
VCC 1.85 Voltage Regulator



Micro Star Restricted Secret

Title	AGP Voltage Regulators	Rev
Document Number	MS-6337	50B
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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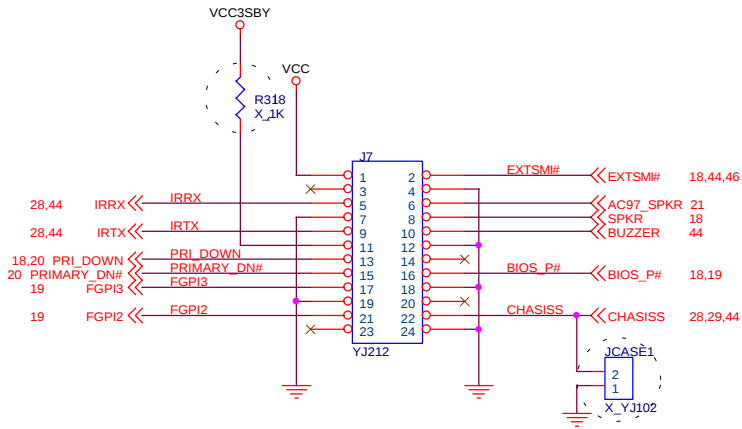
Front Panel and Power Connector



Micro Star Restricted Secret

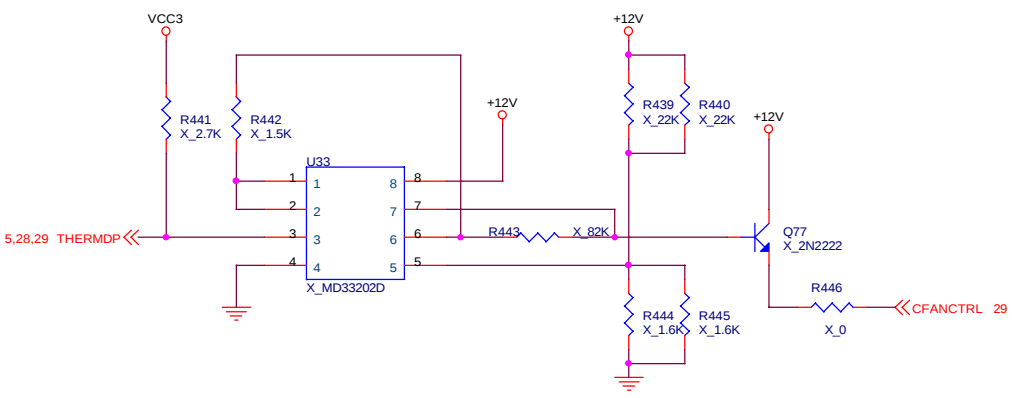
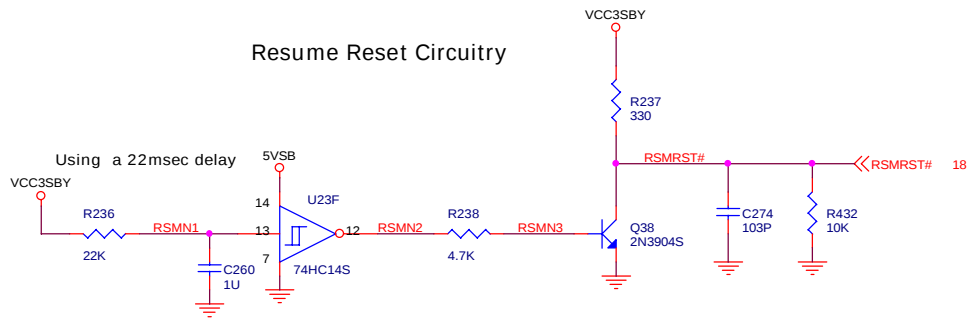
Title	Front Panel and ATX Power Connector	Rev
Document Number	50B	
MS-6337		
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Front Panel



- J7(13-15) For Onboard Codec
- J7(21-23) For FWH GPI
- J7(14) For Smart DLED Language
- J7(16-18) For BIOS Protection

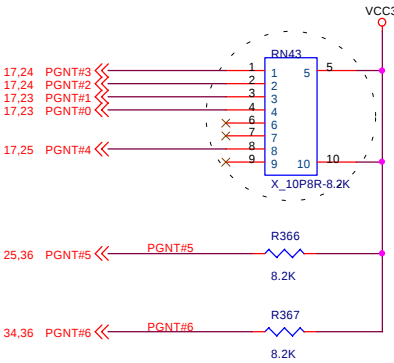
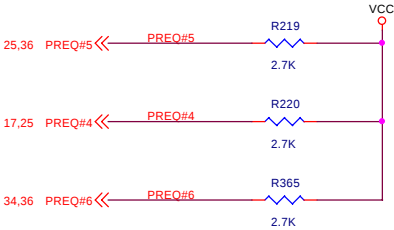
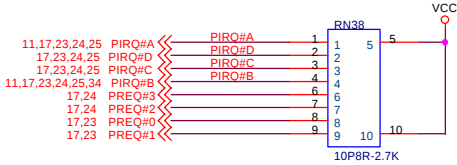
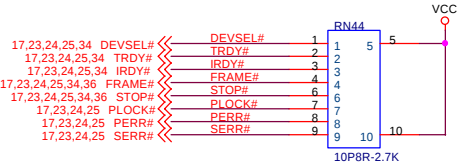
Resume Reset Circuitry



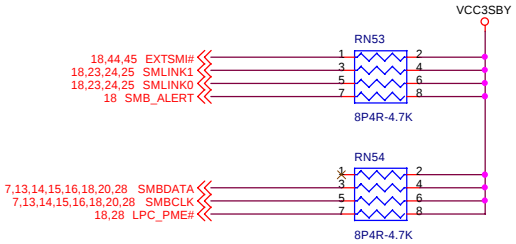
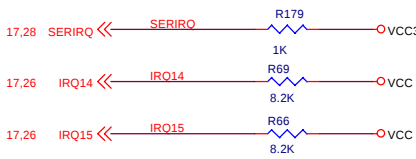
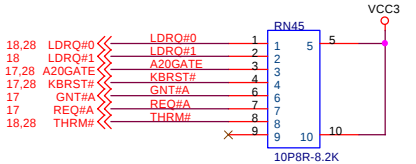
Micro Star Restricted Secret		
Title	Front Panel and ATX Power Connector	Rev
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PULL-UP RESISTORS

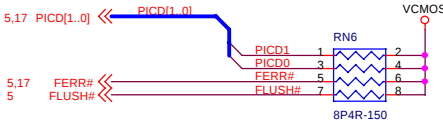
PCI BUS



ICH



CPU



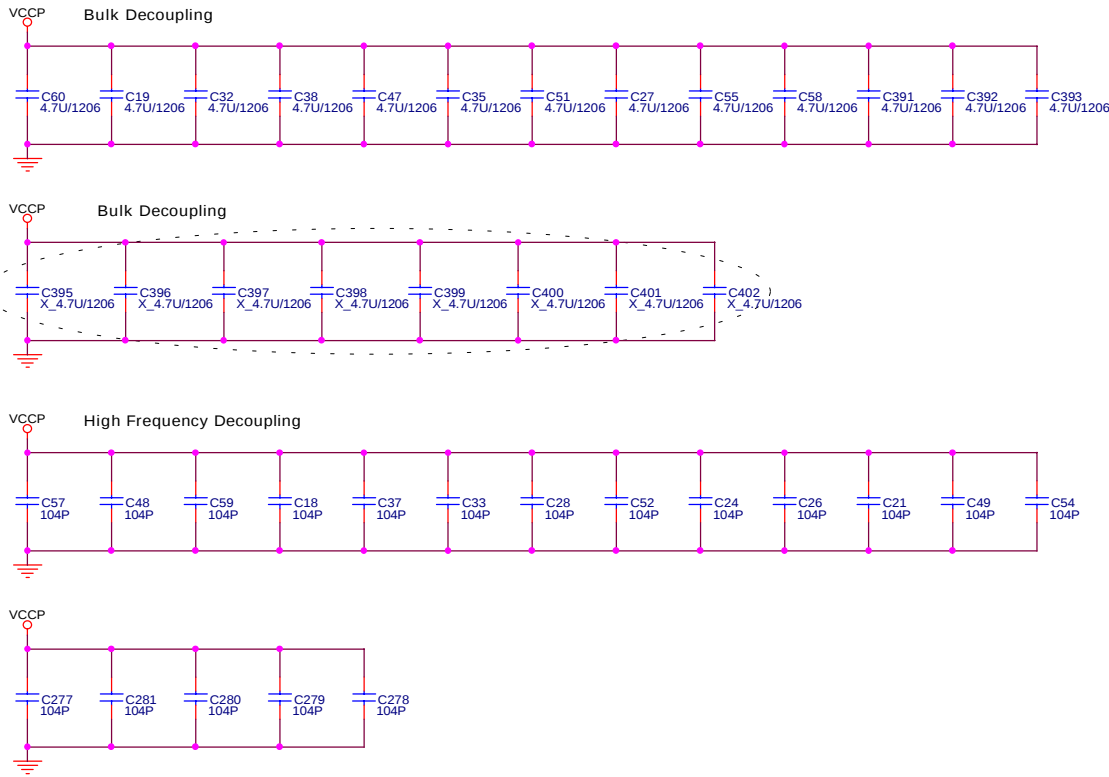
Micro Star Restricted Secret

Title	Pull-Up Resistors	Rev
Document Number	MS-6337	50B
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370-pin Socket Decoupling

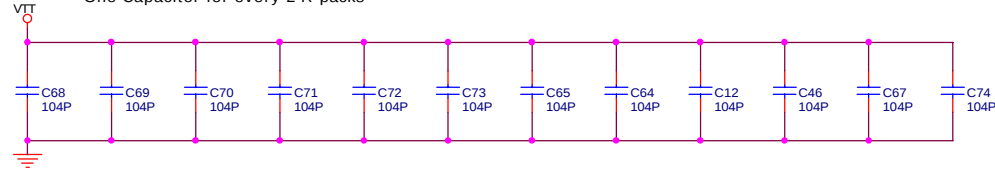
VCC_CORE DECOUPLING

Place in 370 PGA Socket Cavity



VTT DECOUPLING

0603 Package placed within 200mils of VTT Termination R-packs
One Capacitor for every 2 R-packs



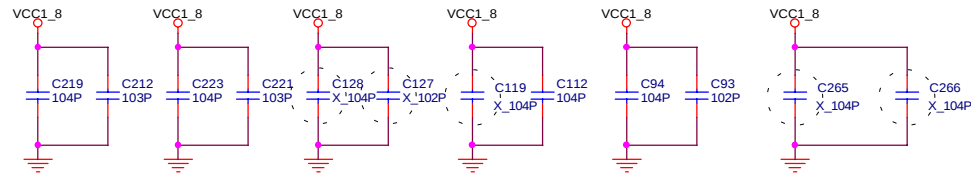
Micro Star Restricted Secret

Title	VRM Decoupling	Rev
Document Number	MS-6337	50B
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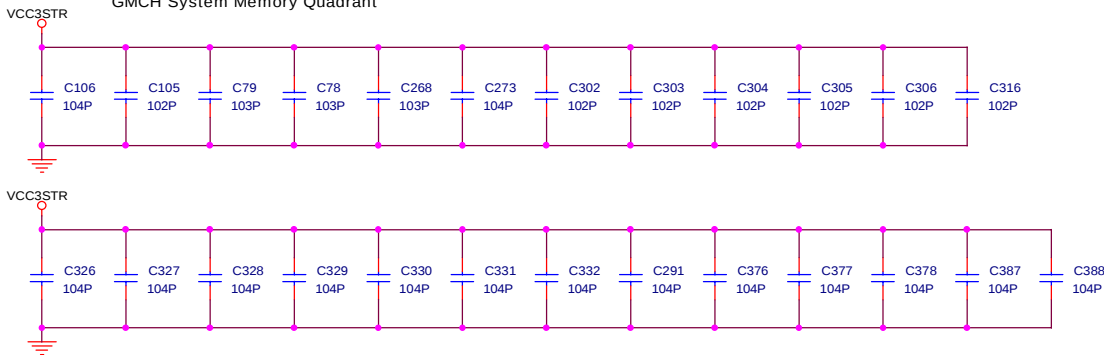
DRAM, Chipset, and BULK Power Decoupling

GMCH Decoupling

GMCH Core Plane Decoupling

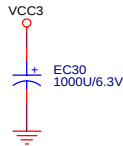


Distribute as close as possible to GMCH System Memory Quadrant

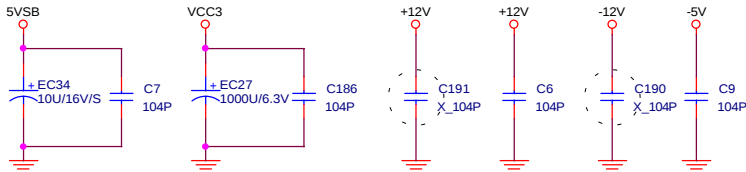


AGP Decoupling

Distribute near the power pins of both SDRAM components

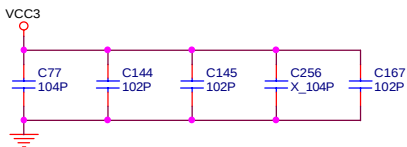


Bulk Power Decoupling

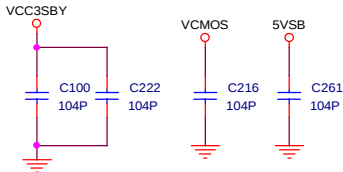


ICH2 Decoupling

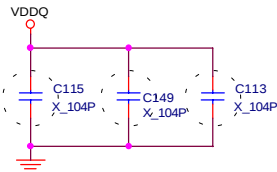
ICH2 3.3V Plane Decoupling:



Distribute near the 3.3V standby power pin of the ICH

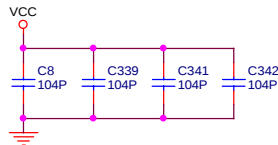


GMCH 3.3V IO Decoupling:
Place near GMCH AGP interface Quadrant

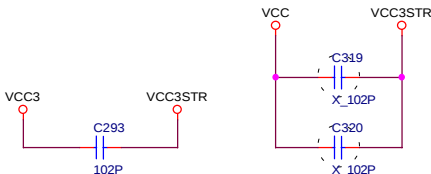
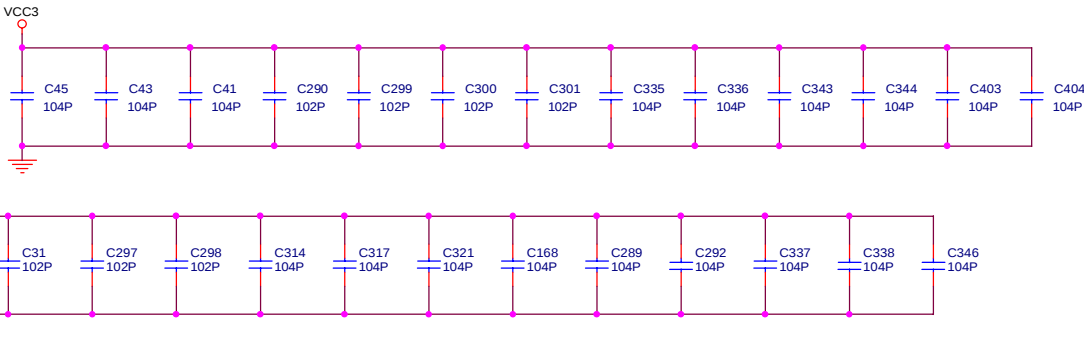
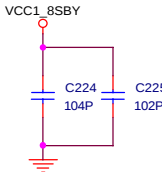


Use surface mount caps placed closed as possible to power pins with short, wide direct connections.

Distribute near the VCC power pin of the LPC



Distribute near the 1.8V standby Power pin of the ICH



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Title	DRAM, ICH, and GMCH Decoupling	Rev
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Revision History

Revision History (Changes from Rev 0A)

Sheet	Description
5	Stuff R37 (330 ohms) for signal PREQ#. Reversed JVT1 that is for up 1 GHz CopperMine processor.
7	Reserved R255 and R254 for REALTEK clock generator RTM560-25R. Swapped signals PCICLK4 and PCICLK5. Delete SW2 and R57, and change RN42 to R251(1K ohms) for signal BSEL0#, and add R252 and R253 (8.2K ohms) pull-down strapping resistors for clock gen FS2 and FS0. Changed SDRAM serial damping RN34, RN35, and RN37 from 22 ohms to 10 ohms R-pack for clock quality. Changed clock 48MHz serial damping RN36 from 22 ohms to 10 ohms for clock quality. Changed CPU and GMCH host clock serial damping R152 and R153 from 33 ohms to 10 ohms for clock quality. Changed clock 66MHz serial damping RN39 from 33 ohms to 22 ohms for clock quality. Changed clock 14MHz serial damping R149, R150 and R242 from 33 ohms to 22 ohms for clock quality. Reserved SDRAM clock bypass CN10, CN11 and CN13 (10pF).
8	Changed GTLREF decoupling capacitor from to 0.1uF.
9	Swapped GMCH reset strap connected RN20.
13~16	Swapped SDRAM clock. Changed SDRAM data and data mask routing.
18	Changed signal VBIAS external capacitor from 2200pF to 0.047uF for RTC accuracy. Removed RN49 (8.2K ohms), and added R269 (8.2K ohms) for GPIO18. Deleted signals MANUSET (GPIO4) and SETVID (GPIO24). Changed signal ATADET1 connect to GPIO4 instead of GPIO2, and GPIO2 connected to RN46. Changed signal NOGO connected to GPIO22 instead of GPIO18. Added signals STRCTRL (GPIO24), KBVCC_CTRL (GPIO25), AUDIO_CTRL1 (GPIO27), and AUDIO_CTRL2 (GPIO28).
21	Changed audio codec to support SigmaTel STAC9708 4-channel and ICE 1236 6-channel.
22	Changed audio codec to support SigmaTel STAC9708 4-channel and ICE 1236 6-channel.
33	Removed L1 and CP1. Added KB/MS VCC control circuit replaced JKBV1, R1 and R2.
34	Added pull-up resistor R271 (4.7K ohms) to VCC3 for ISA HS1 signal.
37	Removed ISA signal NOGO pull-up resistor R206.
38	Changed RN47 to 220 ohms for LED. Reversed LED4, LED5, LED6 and LED1 for definition.
40	Removed Vcore setting page. Removed JSTR1 jumper. Added signal STRCTRL connected to Q4 for DRAM voltage control. Changed VR2 voltage input from 5VSTR to 5VSB. Changed R42 voltage input from VCC1_8SBY to 5VSTR and R42 changed to 300 ohms and R43 changed to 100 ohms. Changed EC32 from 1000uF/6.3V to 10uF/16V SMD.
42	Reserved JGL1 header.
46	Removed C75, C76, C211, C237, C238, C253, C233, C210, C218, C192, C86, C123, C133, C29, C39, C96, C61, C66, C62, C82, C85, and C254.

Revision History (Changes from Rev 0B)

Sheet	Description
4	Changed VIDA[3:0] pull up R-pack 8.2K ohms to VCC.
5	Changed VIDA4 puul up resistor 8.2K ohms to VCC. Added C275 4.7uF/0805 for CPU CLKREF. Added SW1, R297 and R298 for signal BSEL0# and BSEL1# for overclocking.
7	Removed R231. Added four power pin bypass .1uF C269, C270, C271 and C272. Reserved R285 pull down straping for Winbond clock gen mode select. Reserved R286 to PCIRST# signal for Winbond clock gen.
8	Changed C80, C81 to .1uF/0603. Changed C104 to .1uF and C95 to 4.7uF/0805.
9	Added R278 56K ohms pulled up for GMCH power up straps. Added R284 10K ohms pulled down for GMCH power straps.
18	Changed signals ATADET0 and ATADET1 to GPIO6 and GPIO7 instead of GPIO3 (PIRQF#) and GPIO4 (PIRQG#). Changed pulled up RN46 to 2.7K ohms for ICH2 PIRQE# ~ PIRQH#.
22	Added R276 and R277 for Sigmatel 9708 4 channel function.
26	Reserved C283 and C282 10pF to signals IDEACTP# and IDEACTS# for EMI. Changed pulled up RN59 of signal PCIRST# from 8.2K ohms to 1K ohms.
37	Added R275 4.7K ohms for signals NOGO pulled up.
38	Changed DLED pulled up R-pack RN47 and RN58 from 220 ohms to 330 ohms. Added RN76, RN77 and R306 for REALTEK RTA26301.
39	Added R287 and R288 (4.7 ohms) to reduce mosfet gate noise. Added R289 and R290 (10m ohms) for current protect. Added EC39 1500uF/6.3V for Vcore. Changed R25 from 1K ohms 1% to 3.01K ohms 1% for Vcore transient.
40	Added Vcore setting circuits.
41	Changed VR1 from US1150 to 1084, and removed the control circuits for US1150. Added R279 and R280 (4.7K ohms) pulled up to VCC3 for ICH2 GPIO19 and GPIO20. Changed R52 and R59 pulled up from VCC to +12V for NMOS. Changed R49 from 2.94K ohms 1% to 2.43K ohms 1%. Changed R58 from 1.33K ohms 1% to 1.18K ohms 1%.
43	Added R281, R282 and R283 for ICH2 power good.
44	Changed R237 from 10k ohms to 330 ohms and added C274 .01uF to reduce RSMRST# noise.

Revision History

Revision History (Changes from Rev 1)

Sheet	Description
7	Changed R242 from 22 ohms to 47 ohms for signal ICH14M for EMI. Stuffed C169, C170 (10pF), CN10, CN11, CN13 (8P4C-10pF), and C174 (4.7pF) for EMI.
9	Removed power straps R284 for signal SM_MAA11.
12	Stuffed CN5 (8P4C-100pF) for EMI.
17	Changed R174 from 150 ohms to 200 ohms.
18	Removed signal FAN_CTRL and changed VCORE to GPIO21.
20	Added C295 (104pF) close to U21 power pin 14 for EMI.
21	Stuffed C139 and C141 (470pF) for LINE_IN for EMI.
22	Stuffed C134 and C135 (180pF) for SPEAKER for EMI. Changed R276 and R277 from 0 ohms to 10K ohms for audio THD+N quality. Stuffed C136, C137 and C140 (102pF) for EMI.
26	Added C307 and C308 (33pF) for EMI.
29	Removed R28 and signal FAN_CTRL.
31	Removed L12 and CP3 for ground level layout.
32	Stuffed CN9 (8P4C-270pF), C124 and C125 (270pF) for EMI.
38	Changed post voice circuit to REALTEK.
39	Reserved R294, and changed R296 to 68 ohms and R295 to 10K ohms for VCORE transient.
41	Added EC41 (10uF/16V SMD), C284 and C285 (1uF) to regulator 1084 adj pin for improving ripple rejection.
43	Added C294, C15 and C44 (102pF) for EMI.
44	Added C310 and C311 (100pF) for EMI. Reserved C315 (100pF) for EMI. Changed J7 SPEAKER pin out for post voice DLED.
46	Changed C60, C19, C32, C38, C47, C35, C51, C27, C55 and C58 from 4.7uF/0805 to 4.7uF/1206 for VCORE transient.
47	Added C302, C303, C304, C305, C306 and C316 (102pF) to VCC3STR decoupling. Added C289, C290, C299, C300 and C301 (102pF) for VCC3 decoupling. Added C297, C298 (102pF), C314, C317 and C321 (104pF) for VCC decoupling. Reserved C319 and C320 (102pF) cross VCC to VCC3STR. Added C291, C292 and C293 (102pF) from VCC3 cross to VCC1_8, VCC and VCCSTR.

Revision History (Changes from Rev 1.0A)

Sheet	Description
12	Added LC circuit to CRT R,G,B signals for EMI.
18	Added JBAT2 1X3 header and R325 for clearing 627HF keyboard password. Added a resister R322 shorting JBAT1 pin 1 and pin 2. Connected GPIO28 to CNR signal PRIMARY_DN# to fit to CNR spec 1.0.
19	Added three pulled up resistors to FWH GPIO, GPI1 and GPI4.
20	Changed CNR signal PRIMARY_DN# detected circuit to conform to CNR spec 1.0.
21	Added smart DLED post speech output to codec PC_BEEP pin.
28	Added a capacitor C340 104pF for 5VSB decoupling.
30	Reserved CN20 and CN21 180pF for parallel port EMI.
32	Stuffed C129 (102pF) for EMI.
38	Reserved smart DLED 8 languages supported. Added smart DLED post speech output to codec PC_BEEP pin.
47	Added VCC decoupling C337, C338, C345, C346, C339, C341, and C342 (104pF) for EMI. Added VCC3 decoupling C335, C336, C343, and C344 (104pF) for EMI. Added VCC3STR decoupling C326, C327, C328, C329, C330, C331 and C332 (104pF) for EMI.

Revision History (Changes from Rev 3.0)

Sheet	Description
5	Reserved pull-up resistors R357 and R358 for processor BSEL#.
6	Changed CPU Rtt RN17, RN16, RN15, RN18, RN10, RN9, RN5, RN8, RN14, RN13, RN12, RN11, RN19, and RN7 from 10P8R-68 ohms to 10P8R-56 ohms. Changed signal BREQ# pull-down resistor R30 from 68 ohms to 56 ohms.
7	Changed crystal 14.31818 MHz Y1 from CL=16pF to CL=32pF, and added C194 and C202 22pF for frequency 14.31818 MHz accuracy. Reserved R254, R359 and R360, added R361, R362 for Realtek clock generator.
9	Added SM_MAA4~7, SM_MAB4~7 and SM_MAC4~7 serial resistors RN102, RN103 and RN101 8P4R-10 ohms.
10	Reserved signal OCLOCK serial resistor R100 and added signal RCLOCK pull-down resistor C116 8.2k ohms for 815EP MCH. Added signal TVCLKIN pull-up resistor R376 8.2k ohms to VCC1.8 for 815EP MCH. Added signal DOTCLK and IWASTE pull-down resistors C111 and R377 8.2k ohms for 815EP MCH. Changed signal IREF pull-down resistor R80 from 174 ohms 1% to 8.2 kohms for 815EP MCH.
13	Changed DIMM1~4 clock routing.
26	Added R65 and R68 10 kohms for harddisk active led.
27	added R385 and R386 0 ohm for PC to PC networking controller.
28	Reserved IO 627HF clock staps R378 4.7k ohms.
34	Added R380 5.1 ohms / 0805 for IDE RAID pin 117 analog VCC. Changed the INT# and IDSEL of IDE RAID for compaliability.
36	Removed signals SMBDATA and SMBCLK connecting to U29 pin 13 and pin 16.
37	This page is added for USB PC to PC networking circuit.
38	Changed R308 from 61.9k ohms 1% to 33k ohms 1% for post speech intrnal frequency. Added header J13 and R379 for post speech speaker output connecting to chassis speaker.
43	Short C369 for PC beep to buzzer. Disconnected signal SPEAKR to JFP1 pin 13.

Revision History (Changes from Rev 3.0B)

Sheet	Description
	Supported Tualatin Universal Motherboard designed.

Revision History (Changes from Rev 5.0)

Sheet	Description
6	Added Thermtrip# circuit for Tualatin processor.
11	Corrected AGP1 pin C1 and C3 connected to VCC3.
36	Connected PCI clock into MS-1.

Revision History

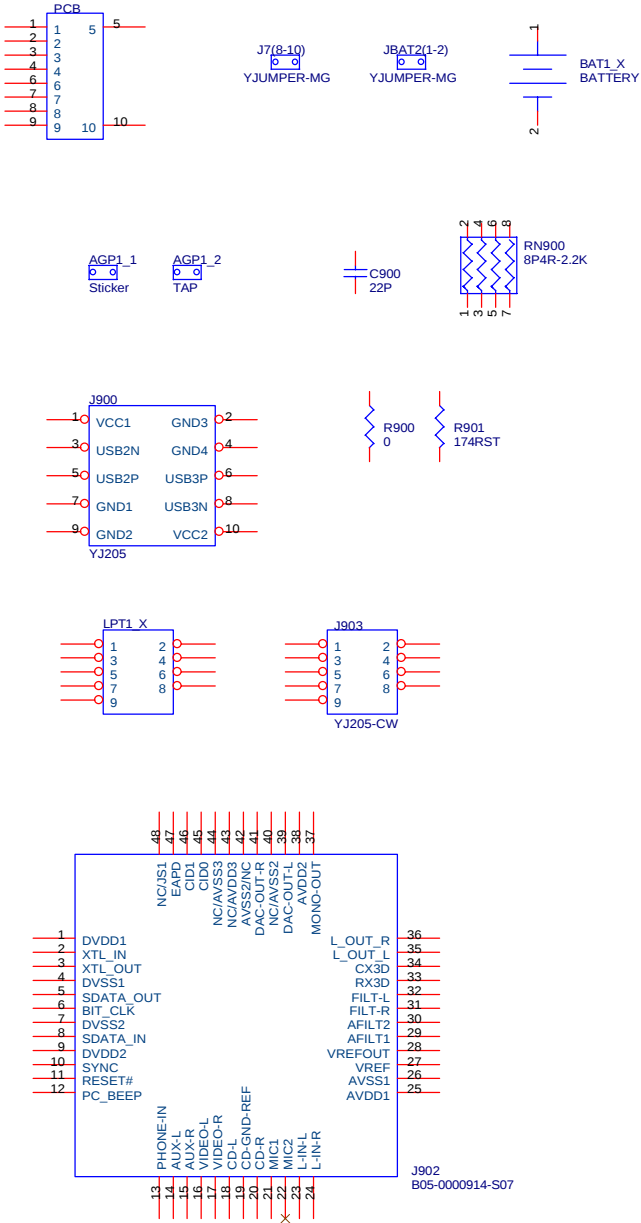
Revision History (Changes from Rev 5.0A)

Sheet	Description
5	Added TCK circuit for Tualatin processor Thermtrip# erratum.
6	Added CPURST# to gate Thermtrip# assertion.
7	Changed clock generator Vtt power good connected to VTPWRGD12.
- - -	Changed 48MHz damping R-pack and bypass C-pack to discrete resistor and cap.

Micro Star Restricted Secret

Title	HISTORY	Rev
Document Number	MS-6337	50B
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AutoBOM Manual Parts



KEY	
B1	AGP_OVRCNT#
B2	5V_A
B3	5V_B
B4	AGP_USB+
B5	GND_Q
B6	INTB#
B7	AGPCLK_CONN
B8	REQ#
B9	VCC3_3_R
B10	ST0
B11	ST2
B12	RBF#
B13	GND_R
B14	RESV_L
B15	SBA0
B16	VCC3_3_S
B17	SBA2
B18	SB_STB
B19	GND_S
B20	SBA4
B21	SBA6
B22	RESV_M
B23	GND_T
B24	3_3AUX_1
B25	VCC3_3_T
B26	GAD30
B27	GAD29
B28	VCC3_3_U
B29	GAD27
B30	GAD25
B31	GND_U
B32	AD_STB1#
B33	GAD23
B34	VDDQ_F
B35	GAD21
B36	GAD19
B37	GND_V
B38	GAD17
B39	C/BE#2
B40	VDDQ_G
B41	IRDY#
B42	3_3AUX_2
B43	GND_W
B44	RESV_N
B45	VCC3_3_I
B46	DEVSEL#
B47	VDDQ_H
B48	PERR#
B49	GND_N
B50	SERR#
B51	C/BE#1
B52	VDDQ_I
B53	GAD14
B54	GAD12
B55	GND_Y
B56	GAD10
B57	GAD8
B58	VDDQ_J
B59	AD_STB0
B60	GAD7
B61	GND_Z
B62	GAD5
B63	GAD3
B64	VDDQ_K
B65	GAD1
B66	VREFCG
KEY	
F1	RESV_O
F2	RESV_P
F3	GND_AA
F4	GND_BB
F5	GND_CC
F6	GND_DD
F7	GND_EE
F8	GND_FF
F9	GND_GG
F10	GND_HH
F11	GND_II
F12	GND_JJ
F13	GND_KK
F14	GND_LL

KEY	
C1	VCC3_3_A
C2	VCC3_3_K
C3	VCC3_3_B
C4	GND_B
C5	GND_C
C6	GND_D
C7	GND_E
C8	GND_F
C9	RESV_A
C10	RESV_B
KEY	
A1	VCC_12V_A
A2	TYPEDT#
A3	RESV_C
A4	AGP_USB-
A5	GND_G
A6	INTA#
A7	RST#
A8	GNT#
A9	VCC3_3_E
A10	ST1
A11	RESV_D
A12	PIPE#
A13	GND_H
A14	WB#
A15	SBA1
A16	VCC3_3_F
A17	SBA3
A18	SB_STB#
A19	GND_I
A20	SBA5
A21	SBA7
A22	RESV_E
A23	GND_J
A24	RESV_F
A25	VCC3_3_G
A26	GAD30
A27	GAD28
A28	VCC3_3_H
A29	GAD26
A30	GAD24
A31	GND_K
A32	AD_STB1#
A33	C/BE#3
A34	VDDQ_A
A35	GAD22
A36	GAD20
A37	GND_L
A38	GAD18
A39	GAD16
A40	VDDQ_B
A41	FRAME#
A42	RESV_G
A43	GND_M
A44	RESV_H
A45	VCC3_3_I
A46	TRDY#
A47	STOP#
A48	PME#
A49	GND_N
A50	PAR
A51	GAD15
A52	VDDQ_C
A53	GAD13
A54	GAD11
A55	GND_O
A56	GAD9
A57	C/BE#0
A58	VDDQ_D
A59	AD_STB0#
A60	GAD7
A61	GND_P
A62	GAD4
A63	GAD2
A64	VDDQ_E
A65	GAD0
A66	VREFCG
KEY	
E1	RESV_I
E2	RESV_J
E3	VCC_12V_B
E4	VCC_12V_C
E5	VCC_12V_D
E6	VCC_12V_E
E7	VCC_12V_F
E8	VCC_12V_G
E9	VCC_12V_H
E10	VCC_12V_I
E11	VCC_12V_J
E12	VCC_12V_K
E13	VCC_12V_L
E14	VCC_12V_M